TUTORIAL SCHEDULE (11.02.2021)

	Session-1	*Session-2*
09.00 AM – 09.25 AM	***Joining the Meeting Hall***	***Joining the Meeting Hall***
09.30 AM –11.00 AM	Fundamentals of RF/Analog Device Modelling – RLC by ***Mr. Praveen Paul, RF & Analog Mixed Signal Compact Modeling Engineer, GLOBALFOUNDRIES.***	Surviving the electronics revolution requires a digital strategy - ***Mr.Pavan Kumar Nanduri, Senior Application Engineer,Mentor Graphics***
11.00 AM – 11.30 AM	Break	
11.30 AM – 1.00 PM	Fundamentals of RF/Analog Device Modelling – RLC - ***Mr. Varuna AB, Design Enablement group, GLOBALFOUNDRIES***	Surviving the electronics revolution requires a digital strategy - ***Mr.Pavan Kumar Nanduri, Senior Application Engineer,Mentor Graphics***
01.00 PM – 2.00 PM	**LUNCH**	
2.00 PM – 3.30 PM	Introduction to Intel FPGAs and FPGA Accelerators - ***Mr. Padmanaban Kalyanaraman,FPGA University Outreach Program Specialist , Intel's Programmable Solutions Group***	Testing of electronic circuits and chips using DFT Methodologies with Tessent DFT solution – ***Mr. Jai Sehgal, Corporate Application Engineer, Siemens EDA business***
3.30 PM – 4.00 PM	Break	
4.00 PM – 5.30 PM	Introduction to Intel FPGAs and FPGA Accelerators - ***Mr. Padmanaban Kalyanaraman,FPGA University Outreach Program Specialist , Intel's Programmable Solutions Group***	Testing of electronic circuits and chips using DFT Methodologies with Tessent DFT solution – ***Mr. Jai Sehgal, Corporate Application Engineer, Siemens EDA business***

Industry Partner

GLOBALFOUNDRIES

VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

CCIS Springer