VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Academic Staff College(ASC)

In association with School of Electronics Engineering (SENSE)

Cordially invites you to

5 Days FDP (10.00 AM - 4.00 PM)

Online

Faculty Coordinators : **Dr. Abdul Majeed K K, Dr. Vikas Vijayvargiya, Dr. Debashish Dash**

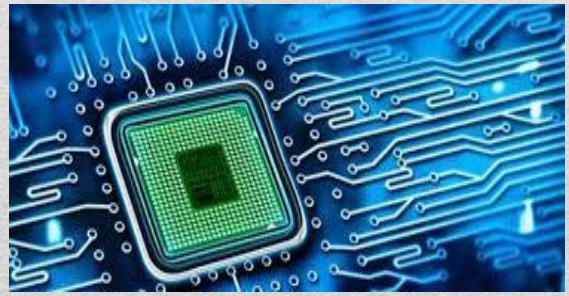
RECENT RESEARCH TRENDS IN VLSI DESIGN (RRTVD-22)

Resource Persons :

- Prof Binsu J Kailath, IIITDM, KANCHEEPURAM.
- Dr Dhanaraj K J, NIT CALICUT.
- Dr Bal Chand Nagar, NIT PATNA.
- Dr Srinivasa Reddy, Modernizechip Solutions, Hyderabad.
- Dr Apurba Chakraborty, BITS Pilani Goa Campus, Goa.
- Dr Sumit Kale, DTU, New Delhi.
- Dr Pooran Singh, Manindra Ecole, Hyderabad.
- Dr Deepika Gupta, IIIT Naya Raipur.
- Dr Bharath Sreenivasulu, Vellore Institute, Chennai.
- Dr Rupam Goswami, Tezpur University, Tezpur.

Discussion Points :

- ✓ Analog Vlsi Design
- ✓ Digital Vlsi Design
- ✓ Device Modelling



21–25, November 2022
(Monday – Friday)

Please register through your vtop login at https://vtop.vit.ac.in/vtop/initialProcess