SCHOOL OF ELECTRONICS ENGINEERING

M. Tech VLSI Design
(M.Tech MVD)

Curriculum
(2019-2020 admitted students)
VISION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

Transforming life through excellence in education and research.

MISSION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

  **World class Education:** Excellence in education, grounded in ethics and critical thinking, for improvement of life.
  **Cutting edge Research:** An innovation ecosystem to extend knowledge and solve critical problems.
  **Impactful People:** Happy, accountable, caring and effective workforce and students.
  **Rewarding Co-creations:** Active collaboration with national & international industries & universities for productivity and economic development.
  **Service to Society:** Service to the region and world through knowledge and compassion.

VISION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

To be a leader by imparting in-depth knowledge in Electronics Engineering, nurturing engineers, technologists and researchers of highest competence, who would engage in sustainable development to cater the global needs of industry and society.

MISSION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

  1. Create and maintain an environment to excel in teaching, learning and applied research in the fields of electronics, communication engineering and allied disciplines which pioneer for sustainable growth.
  2. Equip our students with necessary knowledge and skills which enable them to be lifelong learners to solve practical problems and to improve the quality of human life.
M. Tech VLSI Design

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

1. Graduates will be engineering practitioners and leaders, who would help solve industry’s technological problems.

2. Graduates will be engineering professionals, innovators or entrepreneurs engaged in technology development, technology deployment, or engineering system implementation in industry.

3. Graduates will function in their profession with social awareness and responsibility.

4. Graduates will interact with their peers in other disciplines in industry and society and contribute to the economic growth of the country.

5. Graduates will be successful in pursuing higher studies in engineering or management.

6. Graduates will pursue career paths in teaching or research.
M. Tech VLSI Design

PROGRAMME OUTCOMES (POs)

PO_01: Having an ability to apply mathematics and science in engineering applications.

PO_03: Having an ability to design a component or a product applying all the relevant standards and with realistic constraints, including public health, safety, culture, society and environment

PO_04: Having an ability to design and conduct experiments, as well as to analyse and interpret data, and synthesis of information

PO_05: Having an ability to use techniques, skills, resources and modern engineering and IT tools necessary for engineering practice

PO_06: Having problem solving ability- to assess social issues (societal, health, safety, legal and cultural) and engineering problems

PO_07: Having adaptive thinking and adaptability in relation to environmental context and sustainable development

PO_08: Having a clear understanding of professional and ethical responsibility

PO_11: Having a good cognitive load management skills related to project management and finance
M. Tech VLSI Design

ADDITIONAL PROGRAMME OUTCOMES (APOs)

APO_02: Having Sense-Making Skills of creating unique insights in what is being seen or observed (Higher level thinking skills which cannot be codified)

APO_03: Having design thinking capability

APO_04: Having computational thinking (Ability to translate vast data in to abstract concepts and to understand database reasoning)

APO_07: Having critical thinking and innovative skills

APO_08: Having a good digital footprint
M. Tech VLSI Design

PROGRAMME SPECIFIC OUTCOMES (PSOs)

On completion of M. Tech (VLSI) degree, students will be able to:

PSO1: Apply advanced concepts in Physics of semiconductor devices to design VLSI systems.

PSO2: Design ASIC and FPGA based systems using industry standard tools.

PSO3: Solve research gaps and provide solutions to socio-economic, and environmental problems.
## M. Tech VLSI Design

### CREDIT STRUCTURE

**Category-wise Credit distribution**

<table>
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<tr>
<th>Category</th>
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M. Tech VLSI Design

DETAILED CURRICULUM

University Core

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M. Tech VLSI Design

Programme Core

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## University Elective Baskets

### Management courses

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<tr>
<th>S.No</th>
<th>Course Title</th>
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### Humanities courses
Course Code | Course Title | L | T | P | J | C
--- | --- | --- | --- | --- | --- | ---
ECE5014 | ASIC DESIGN | 3 | 0 | 2 | 0 | 4

Pre-requisite | Nil

Course Objective:
The course is aimed to
1. explain the types of ASIC and typical ASIC design Flow.
2. give the students an understanding of HDL coding guidelines and synthesizable HDL constructs.
3. explain the RTL synthesis Flow with respect to different cost function.
4. teach the various timing parameter and how to perform Static Timing Analysis for ASIC chips.
5. discuss the various abstraction levels in physical design and guidelines at each abstraction level.
6. provide detailed insight on importance of physical design verification.

Expected Course Outcome:
At the end of the course the student will be able to
1. Understand different types of ASICs and design flows.
2. Design digital systems by adhering to synthesizable HDL constructs.
3. Synthesize the given design by considering various constraints and to optimize the same.
4. Understand various timing parameters and compute computation time for a given design using static timing analysis.
5. Perform physical design by adhering to guidelines.
6. Apprehend the importance of physical design verification.
7. Design ASIC based systems using industry standard tools.

Student Learning Outcomes (SLO): 1, 17, 18
1. Ability to apply mathematics and science in engineering applications.
17. Ability to use techniques, skills and modern engineering tools necessary for engineering practice.
18. Critical thinking and innovative skills.

Module:1 | ASIC Design Methodology & Design Flow | 4 hours
--- | --- | ---
Implementation Strategies for Digital ICs: Custom IC Design- Cell-based Design Methodology - Array based implementation approaches - Traditional and Physical Compiler based ASIC Flow.

Module:2 | Verilog HDL Coding Style for Synthesis | 6 hours
--- | --- | ---
HDL Coding style – Guidelines and Recommendation - FSM Coding Guideline and Coding Style for Synthesis.

Module:3 | RTL Synthesis | 8 hours
--- | --- | ---

Module:4 | Timing Parameters | 5 hours
--- | --- | ---

Module:5 | Static Timing Analysis | 7 hours
Timing Analysis - Clock skew optimization – Clock Tree Synthesis.

Module:6  Physical Design  8 hours
Detailed step in Physical Design Flow- Guidelines for Floor plan, Placement and routing. Conducting layers and their characteristics - Cell-based back-end design –ECO – Packaging-
Layout Issues-Preventing electrical overstress.

Module:7  Physical Design Verification  5 hours
Static verification techniques-Post-layout design verification.

Module:8  Contemporary issues:  2 hours

Total Lecture hours:  45 hours

Text Book(s)

Reference Books

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Challenging Experiments (Indicative)
1. Phase- I Design of digital architecture
   Design Specification: Starting with the soda machine dispenser design described in lecture, create a block diagram and high-level state machine for a soda machine dispenser that has a choice of two soda types, and that also provides change to the consumer. A coin detector provides the circuit with a 1-bit input c that becomes 1 for one clock cycle when a coin is detected, and an 8-bit input a indicating the coin’s value in cents. Two 8-bit input s1 and s2 indicate the cost of the two soda choices. The user’s soda selection is controlled by two buttons b1 and b2 that when pushed will output 1 for one clock cycle. If the user has inserted enough change for their selection, the circuit should set either output bit d1 or d2 to 1 for one clock cycle, causing the selected soda to be dispensed. The soda dispenser circuit should also set an output bit cr to 1for one clock cycle if change is required, and should output the amount of change required using on an 8-bit output ca. Use the RTL design method to convert the high-level state machine to a controller and a data path. Design the data path to structure, but design the controller to the point of an FSM only.

   12 hours

2. Phase-II Logical Synthesis of digital architecture
   Apply design and timing constraints :
   DRC constraints are: set_max_fanout, set_max_transition and

   6 hours
<table>
<thead>
<tr>
<th>Phase</th>
<th>Description</th>
<th>Duration</th>
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<td><strong>Phase-III  Netlist Optimization and Formal Verification</strong></td>
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<tr>
<td></td>
<td>Apply power optimization constraints, Gate Level Simulation and Formal</td>
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<tr>
<td></td>
<td>verification of digital architecture.</td>
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<td><strong>Phase-IV Physical Synthesis of digital architecture</strong></td>
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<td>create_floorplan, set_propgated_clock, preroute_standard_cells, set_route_zrt.</td>
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<td>5.</td>
<td><strong>Phase-V Physical Verification of digital architecture</strong></td>
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<td>set_fix_multiple_port_nets, write_physical_constraints and write_parasitics</td>
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**Total Laboratory hours:** 30 hours

Mode of Evaluation: Continuous assessment of challenging experiments /Final Assessment Test (FAT).

Recommended by Board of Studies | 13-12-2015
Approved by Academic Council    | No. 40 | 18-03-2016
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<th>Course Title</th>
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**Pre-requisite**: Nil

**Course Objective:**

The course is aimed to

1. apply the models for state-of-the-art VLSI components, fabrication steps, hierarchical design flow and semiconductor business economics to judge the manufacturability of a design and assess its manufacturing costs.
2. focus on the systematic analysis and design of basic digital integrated circuits in CMOS technology.
3. enhance problem solving and creative circuit design techniques.
4. emphasize on the layout design of various digital integrated circuits.
5. focus on the methodologies and design techniques related to digital integrated circuits.

**Expected Course Outcome:**

At the end of the course the student will be able to

1. Understand design metric and MOS physics
2. Design layout for various digital integrated circuits.
3. Design the CMOS inverter with optimized power, area and timing.
4. Design static and dynamic digital CMOS circuits.
5. Understand the timing concepts in latch and flip-flops.
6. Design CMOS memory arrays.
7. Understand interconnect and clocking issues.

**Student Learning Outcomes (SLO):** 5, 6, 14

5. Having design thinking capability.
6. Having an ability to design a component or a product applying all the relevant standards and with realistic constraints.
14. Having an ability to design and conduct experiments, as well as to analyze and interpret data.

**Module: 1  Introduction:** 3 hours


**Module: 2  Fabrication Technologies:** 7 hours


Fabrication of MOSFET with Metal Gate and Self-aligned Poly-Gate Processes with details on CMOS Design Rules and Layouts, Fabrication of CMOS inverter with details on Design Rules and Layouts.

**Module: 3  The CMOS Inverter:** 5 hours

Static CMOS Inverter- Static and Dynamic Behavioural Practices of CMOS Inverter – Noise Margin.

Components of Energy and Power – Switching - Short-Circuit and Leakage Components.

Technology scaling and its impact on the inverter metrics - Passive and Active Devices.
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<tr>
<th>Module:4</th>
<th>Static &amp; Dynamic CMOS Design:</th>
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<tbody>
<tr>
<td>Complementary CMOS - Ratioed Logic (Pseudo NMOS, DCVSL) - Pass Transistor Logic - Transmission gate logic - Dynamic Logic Design Considerations - Speed and Power Dissipation of Dynamic logic - Signal integrity issues - Domino Logic.</td>
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<th>Module:5</th>
<th>CMOS Sequential Logic Circuit Design:</th>
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<td>Introduction - Static Latches and Registers - Dynamic Latches and Registers - Pulse Based Registers - Sense Amplifier based registers - Latch vs. Register based pipeline structures.</td>
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<th>Designing Memory &amp; Array structures:</th>
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<th>Interconnects and Timing Issues:</th>
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**Text Book(s)**


**Reference Books**


**Mode of Evaluation:** Continuous Assessment Test – I (CAT-I), Continuous Assessment Test – II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

**List of Projects (Indicative)**

1. Design and simulate a 16-bit comparator by using 8T full adders
2. Pass transistor logic based ALU design using low power full adder design
3. Design of high performance power efficient flip-flop using transmission gates
5. Design of current comparator using FINFET
6. Analysis of leakage current and leakage power reduction during reduction in CMOS SRAM cell
7. Design of encoder for a 5GS/S 5 bit flash ADC
8. Design a 65 nm reliable 6T CMOS SRAM cell with minimum size transistors

**Mode of Evaluation:** Review I, II and III

Recommended by Board of Studies 13-12-2015

Approved by Academic Council No. 40 18-03-2016
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Course Objectives:
The course is aimed to
1. analyze and design single-ended and differential IC amplifiers.
2. understand the relationships between devices, circuits and systems.
3. emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.

Expected Course Outcome:
At the end of the course the student will be able to
1. Analyse low-frequency characteristics of single-stage amplifiers and differential amplifiers.
2. Analyse high-frequency response and noise of amplifiers.
3. Understand the feedback concepts.
4. Analyse and Design of High Gain Amplifiers.
5. Understand stability analysis and frequency compensation techniques of amplifiers.
6. Understand the basic concepts, non-idealities and applications of PLLs.
7. Design and characterize amplifiers according to design specifications in Cadence CAD software.

Student Learning Outcomes (SLO): 1, 5, 17
1. Ability to apply mathematics and science in engineering applications.
5. Having design thinking capability
17. Ability to use techniques, skills and modern engineering tools necessary for engineering practice.

Module:1  | Current source and Amplifier design: | 8 hours

Module:2  | Frequency response and Noise analysis of Amplifiers: | 8 hours
Miller effect, Frequency response of Common Source stage, Common Gate stage, Cascode stage and Differential pair. Noise in Amplifiers: Common Source stage, Common Gate stage, Cascode stage, Differential pair. Noise Bandwidth.

Module:3  | Feedback Amplifiers: | 7 hours

Module:4  | Operational Amplifier | 8 hours
Amps, Common-Mode feedback loop stability.

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<th>Module:5</th>
<th>Stability analysis</th>
<th>4 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic Concepts, Instability and the Nyquist Criterion, Stability Study for a Frequency-Selective Feedback Network, Effect of Pole Locations on Stability</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:6</th>
<th>Frequency compensation</th>
<th>4 hours</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>Phase Locked Loops</th>
<th>4 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Problem of Lock acquisition, Phase Detector, Basic PLL and its dynamics, Charge-pump PLL, Non-ideal effects in PLL: PFD/CL non idealities, Jitter, Delay Locked Loop, Applications.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Lecture hours:</td>
<td>45 hours</td>
<td></td>
</tr>
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</table>

Text Book(s)


Reference Books


Mode of Evaluation: Continuous Assessment Test – I (CAT-I) , Continuous Assessment Test – II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Challenging Experiments (Indicative)

<table>
<thead>
<tr>
<th>Experiment</th>
<th>Description</th>
<th>Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Analysis and Design of Common Source Amplifier with Diode Connected Load and Suggest a Circuit to achieve higher gain.</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>Analysis and Design of Common Gate Amplifier with Resistive load and Current Source load. Justify the results in terms of input impedance of the circuit.</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>Analysis and Design of Simple Current Mirror and Suggest a circuit to minimize the error in the output current.</td>
<td>4</td>
</tr>
<tr>
<td>4</td>
<td>Analysis and Design of Differential Amplifier with Active load and Current Source Load.</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>Analysis and Design of Cascode Amplifier and Suggest a Circuit to overcome Voltage Headroom Limitation.</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>Analysis and Design of Two-Stage Opamp with Frequency Compensation.</td>
<td>8</td>
</tr>
</tbody>
</table>

Total Laboratory hours: 30 hours

Mode of Evaluation: Continuous assessment of challenging experiments / Final Assessment Test (FAT).

Recommended by Board of Studies | 13-12-2015
Approved by Academic Council | No. 40 18-03-2016
Course Objectives:
The course is aimed to
1. understand the various abstraction levels in Verilog HDL and thus model tasks & functions at behavioral level.
2. model the state machines using D and JK Flip Flops and design the complex combinational and sequential logic circuits using various constructs in Verilog.
3. understand the types programmable logic devices and building blocks of FPGA and thus implement the design using Xilinx and ALTERA FPGAs.

Expected Course Outcome:
At the end of the course the student will be able to
1. Understand various abstraction levels in Verilog HDL.
2. design finite state machine using D and JK Flip Flop.
3. model sequential circuit using behavioural modelling.
4. Design the complex combinational and sequential logic circuits using various constructs in Verilog.
5. Understand programmable logic devices and various blocks exist in FPGA.
6. distinguish the architectural and resource difference between ALTERA and Xilinx.
7. use EDA tool to design complex combinational and sequential circuits.
8. develop and prototype digital systems design using FPGA.

Student Learning Outcomes (SLO): 1,5,17
1. Ability to apply mathematics and science in engineering applications.
5. Having design thinking capability.
17. Having an ability to use techniques, skills and modern engineering tools necessary for engineering practice.

Module:1 | Verilog HDL – Data Flow & Structural Modeling | 6 hours

Module:2 | State Machine Design | 4 hours

Module:3 | Verilog HDL – Behavioral Modeling | 5 hours
Behavioral level Modeling- Procedural Assignment Statements- Blocking and Non-Blocking Assignments -Tasks & Functions - Useful Modeling Techniques.

Module:4 | Verilog Modeling of Combinational Circuits | 4 hours
Behavioral, Data Flow and Structural Realization of Adders and Multipliers

Module:5 | Verilog Modeling of Sequential Circuits | 4 hours
Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM - FSM Verilog
### Module:6  
**FPGA Architecture**  
3 hours

Types of Programmable Logic Devices: PLA, PAL, CPLD - FPGA Architecture - Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA.

### Module:7  
**Xilinx and ALTERA FPGAs**  
2 hours


### Module:8  
**Contemporary issues:**  
2 hours

Total Lecture hours: 30 hours

#### Text Book(s)


#### Reference Books


#### Mode of Evaluation:
Continuous Assessment Test –I (CAT-I), Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

#### List of Challenging Experiments (Indicative)

1. Many ink-jet printers have six cartridges for different colored ink: black, cyan, magenta, yellow, light cyan and light magenta. A multibit signal in such a printer indicates selection of one of the colors. Write a data flow Verilog model for a decoder for use in the inkjet printer described above. The decoder has three input bits representing the choice of color cartridge and six output bits, one to select each cartridge. Verify the output of the design using test bench by simulating in Modelsim Simulator. Implement the design in ALTERA DE2-115 Board and verify it’s functionality.

2. Write a behavioral Verilog code to divide the ALTERA DE2-115 Board clock frequency 50MHz by 40MHZ, 30MHz, 20 MHz, 10MHz. Display each of the output using LEDs available in the board.

3. Design and implement a circuit on the DE2-115 board that acts as a time-of-day clock. It should display the hour (from 0 to 23) on the 7-segment displays HEX7–6, the minute (from 0 to 60) on HEX5–4 and the second (from 0 to 60) on HEX3–2. Use the switches SW15–0 to preset the hour and minute parts of the time displayed by the clock.

4. We wish to implement a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. There is an input w and an output z. Whenever w = 1 or w = 0 for four consecutive clock pulses the value of z has to be 1; otherwise,
5. Write a behavioral Verilog code to design FIFO with the following specification
   d_in: input data; 8 bit width is considered
   d_out: output data; 8 bit width is considered ·
   w_en: write enable signal
   r_en: read enable signal
   w_next_en: read next enable
   r_next_en: write next enable
   w_clk: write clock; 10 MHz for this design
   r_clk: read clock; 50 MHz for this design
   w_ptr: write address pointer; 4 bit to address depth of 16 ·
   r_ptr: read address pointer; 4 bit to address depth of 16 ·
   ptr_diff: address pointer difference; 4 bit width
   f_full_flag: FIFO full flag; asserted when FIFO is full ·
   f_empty_flag: FIFO empty flag; asserted when FIFO is empty

   Use Dual Port RAM available in ALTERA IP library to realize the FIFO. Implement the design using ALTERA DE2-115 board.

Total Laboratory hours: 30 hours

Mode of Evaluation: Continuous assessment of challenging experiments / Final Assessment Test (FAT).

List of Projects (Indicative)

1. Design MIPS 32-Bit RISC Processor and implement it using ALTERA Cyclone IV FPGA and study about it’s performance.
2. Design a Reconfigurable FIR Filter and verify it’s functionality through test bench. Implement the design using ALTERA Cyclone IV FPGA.
3. Design and Implementation of Smart Traffic Light System for congested four way road using ALTERA Cyclone IV FPGA.
4. Design and Implementation of CORDIC Algorithm using ALTERA Cyclone IV FPGA.

Mode of Evaluation: Review I, II & III

Recommended by Board of Studies 13-12-2015
Approved by Academic Council No. 40 18-03-2016
Course code | Physics of VLSI Devices | L | T | P | J | C  
---|---|---|---|---|---|---  
ECE 5018 | | 3 | 0 | 0 | 0 | 3  
Pre-requisite | None | Syllabus version | v.1.1  

**Course Objectives:**  
The course is aimed to  
1. Expound the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration, modeling and physics of various carrier current transport mechanisms  
2. Introduce detailed physics and modeling of PN Junction, MOS capacitors, and MOSFETs  
3. Review and discuss in detail the short channel effects and the issues of UDSM transistors  

**Expected Course Outcome:**  
At the end of the course the student will be able to  
1. Design extrinsic semiconductors with specific carrier concentrations and, understand the band structure and diagrams of semiconductors.  
2. Calculate and model the carrier transport mechanism in semiconductors.  
3. Model PN-junctions of given specifications  
4. Model MOS capacitors  
5. Model MOSFETs and model the MOSFETs  
6. Mitigate the short channel effects and design UDSM transistors  

**Student Learning Outcomes (SLO):**  
1. Having an ability to apply mathematics and science in engineering applications  
5. Having a clear understanding of the subject related concepts and of contemporary issues  
17. Having an ability to use techniques, skills and modern engineering tools necessary for engineering practice  

**Module: 1 | Semiconductor Physics | 5 hours**  

**Module: 2 | Carrier Transport in Semiconductors | 4 hours**  
Current flow mechanisms: Drift current, Diffusion current - Mobility of carriers - Current density equations - Continuity equation.  

**Module: 3 | P-N Junctions | 5 hours**  
Thermal equilibrium physics - Energy band diagrams - Space charge layers - Poisson equation - Electric fields and Potentials - p-n junction under applied bias - Static current-voltage characteristics of p-n junctions - Breakdown mechanisms.  

**Module: 4 | MOS Capacitor | 8 hours**  
Accumulation - Depletion - Strong inversion - Threshold voltage - Contact potential - Gate work function - Oxide and Interface charges - Body effect - C-V characteristics of MOS  

**Module: 5 | MOSFETs and Compact Models | 8 hours**  
Drain current - Saturation voltage - Sub-threshold conduction - Effect of gate and drain voltage on carrier mobility - Compact models for MOSFET and their implementation in SPICE: Level 1, 2
and 3 - MOS model parameters in SPICE.

<table>
<thead>
<tr>
<th>Module:6</th>
<th>Scaling and Short Channel Effects</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Effect of scaling - Channel length modulation - Punch-through - Hot carrier degradation - MOSFET breakdown - Drain-induced barrier lowering.</td>
</tr>
<tr>
<td></td>
<td>6 hours</td>
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</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>UDSM Transistor Design Issues</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>Effect of tox - Effect of high-k and low-k dielectrics on the gate leakage and Source and drain leakage - tunneling effects - Different gate structures in UDSM - Impact and reliability challenges in UDSM.</td>
</tr>
<tr>
<td></td>
<td>7 hours</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>2 hours</td>
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</table>

| Total Lecture hours: | 45 hours |

**Text Book(s)**


**Reference Books**


**Mode of Evaluation:** CAT / Assignment / Quiz / FAT

**Recommended by Board of Studies:** 05-10-2017

**Approved by Academic Council:** No. 47 05-10-2017
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<th>P</th>
<th>J</th>
<th>C</th>
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<tr>
<td>ECE5019</td>
<td>COMPUTER AIDED DESIGN FOR VLSI</td>
<td>3</td>
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<td>3</td>
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<tr>
<td>Pre-requisite</td>
<td>Nil</td>
<td></td>
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</tbody>
</table>

**Course Objective:**

The course is aimed to

1. imbibe the students with the fundamentals of graphs, the relevance and, their applications to VLSI design automation.
2. introduce the students with relevant examples the estimation of computational complexity and the general classes of computational problems.
3. explain With relevant examples and algorithms demonstrate partitioning, floor planning, area routing, clock routing and pin assignment of physical design flow.

**Expected Course Outcome:**

At the end of the course students will be able to

1. Formulate the graphs for the given problems;
2. Calculate and analyse the computational complexity of physical design algorithms;
3. Partition a given design.
4. Express and change the floorplans in an abstract manner and use computer algorithms to make large and optimized floorplans.
5. Make optimized placements on the silicon chip and perform complex routing using algorithms and computer codes.
6. Design clock trees to distribute the clock signals on the chip while satisfying various constraints like clock skew and wire length.

**Student Learning Outcomes (SLO):**

1. Having an ability to apply mathematics and science in engineering applications
6. Having an ability to design a component or a product applying all the relevant standards and with realistic constraints

**Module:1**  **Introduction to course**  **5 hours**

Y Chart- Physical design top down flow- Review of graph theory: complete graph, connected graph, sub graph, isomorphism, bi partite graph tree.

**Module:2**  **Computational complexity of algorithms**  **4 hours**

Big-O notation- Class P- class NP -NP-hard- NP-complete.

**Module:3**  **Partitioning**  **6 hours**

Problem formulation- Group Migration Algorithm: Kernighan-Lin Simulated annealing based Partitioning.

**Module:4**  **Floor planning**  **6 hours**

Stock Meyer algorithm- Wong-Liu algorithm (Normalized polish expression)- Integer Linear Programming (ILP) based floor planning.

**Module:5**  **Pin Assignment and Placement**  **7 hours**

Pin Assignment: Concentric circle mapping, Topological pin assignment- Power and ground
routing.
Placement: Wire length estimation models for placement - Quadratic placement- Sequence pair technique.

<table>
<thead>
<tr>
<th>Module:6</th>
<th>Routing</th>
<th>8hours</th>
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</thead>
</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>Clocking Tree Topologies</th>
<th>7hours</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tbody>
</table>

**Total Lecture hours:** 45hours

**Text Book(s)**

**Reference Books**

Mode of Evaluation: Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

**Recommended by Board of Studies** 13-12-2015

**Approved by Academic Council** No. 40 18-03-2016
### Course Objective:

The course is aimed to

1. Explore different Digital Signal Processor (DSP) architectures and to design systems using programmable DSPs.
2. Improve system performance using different pipelining techniques, processor array and systolic array.
3. Interface of memory and peripherals to a DSP; and acquire knowledge on different codec implemented on DSP.

### Expected Course Outcome:

The students will be able to

1. Identify and use specific Digital Signal Processor for various applications.
2. Design a system using programmable DSP.
3. Implement pipelining techniques to improve system performance.
4. Implement applications using processor array and systolic arrays to enhance the performance.
5. Design involving memory and other interfaces to DSP.
6. Design of various codecs on target DSPs.

### Student Learning Outcomes (SLO): 1,17

1. Ability to apply mathematics and science in engineering applications.
17. Ability to use techniques, skills and modern engineering tools necessary for engineering practice

#### Module:1  DSP Integrated Circuits and VLSI Technologies 2 hours

Standard digital signal processors - Application specific IC’s for DSP - DSP systems - DSP system design - Integrated circuit design.

#### Module:2  Architectures for programmable DSP 4 hours

Basic Architectural Features - DSP Computational Building Blocks - Bus Architecture and Memory - Data Addressing Capabilities - Address Generation Unit - Programmability and Program Execution - Features for External Interfacing.

#### Module:3  Execution Control and Pipelining 4 hours

Hardware looping – Interrupts – Stacks - Relative Branch support - Pipelining and Performance - Pipeline Depth – Interlocking - Branching effects - Interrupt effects - Pipeline Programming models.

#### Module:4  Synthesis of DSP Architectures 6 hours


#### Module:5  Interfacing Memory and I/O to DSP Processors 5 hours
External bus interfacing signals - Memory interface - Parallel I/O interface - Programmed I/O - Interrupts and I/O - Direct memory access (DMA) A Multichannel buffered serial port (McBSP) - McBSP Programming.

<table>
<thead>
<tr>
<th>Module:6</th>
<th>Interfacing CODEC</th>
<th>3 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>CODEC interface circuit - CODEC programming - A CODEC-DSP interface example.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>Multiprocessor Systems</th>
<th>4 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architectures of Multiprocessors - Performance comparison of - Multiprocessor Structures.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>(\text{Total Lecture hours:} \quad 30) hours</td>
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</table>

Text Book(s)

Reference Books

Mode of Evaluation: Continuous Assessment Test – I (CAT-I), Continuous Assessment Test – II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Projects (Indicative)
1. Image Compression algorithm implementation in Programmable DSP.
2. Image processing algorithm implementations on FPGA.
3. Turbo Decoder implementation.
4. CORDIC Algorithm implementation in PDSP/FPGA/ASIC flow.
5. Improved Adaptive filters.
6. Improved Median filters.

Mode of Evaluation: Review I, II and III
Recommended by Board of Studies 13-12-2015
Approved by Academic Council No. 40 18-03-2016
<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>J</th>
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<tbody>
<tr>
<td>ECE5022</td>
<td>VLSI DIGITAL SIGNAL PROCESSING</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

**Pre-requisite**: Nil

**Course Objective**: The course aimed to:
1. Familiarise various representation methods of DSP algorithms, understand the significance of the iteration bound and to calculate the same for a given single-rate and/or multi-rate DFG.
2. Understand and apply the architectural transformation techniques such as retiming, unfolding and folding on a given DFG.
3. Introduce the algorithmic and numerical strength reduction methods for performance improvement.
4. Signify and calculate the effects of scaling and round-off noise for a given digital filter with limited word length.

**Expected Course Outcome**: The students will be able to:
1. Compare various representation methods of DSP algorithms.
2. Find iteration bound of a given single and/or multi-rate DFG.
3. Understand and transform the given DFG using retiming with constraints.
4. Apply unfolding and folding transformations on the given DFG.
5. Understand and apply algorithmic and numerical strength reduction methods.
6. Understand and calculate scaling and round-off noise of the given digital filter with limited word length.

**Student Learning Outcomes (SLO)**: 1, 9
1. Ability to apply mathematics and science in engineering applications.

**Module: 1 Introduction to Digital Signal Processing**  5 hours
Typical DSP Algorithms - DSP Application Demands andScaled CMOS Technologies - Representations of DSP Algorithms - Data-Flow Graph Representations.

**Module: 2 Iteration Bound**  5 hours

**Module: 3 Pipelining, Parallel processing and Retiming**  8 hours

**Module: 4 Unfolding**  6 hours

**Module: 5 Folding**  6 hours
Introduction, Folding Transformation, Register Minimization Techniques, Register Minimization.
Introduction to Algorithmic Strength Reduction, Cook-Toom Algorithm, Iterated Convolution, Cyclic Convolution, Discrete Cosine Transform. Introduction to Numerical Strength Reduction, Canonic Signed Digit Arithmetic, Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression Sharing in Digital Filters.

<table>
<thead>
<tr>
<th>Module:6</th>
<th>Algorithmic &amp; Numerical Strength Reduction</th>
<th>7 hours</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>Scaling and Rounding Noise</th>
<th>6 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Module:8</td>
<td>Contemporary issues:</td>
<td>2 hours</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Total Lecture:</th>
<th>45 hours</th>
</tr>
</thead>
</table>

**Text Book(s)**


**Reference Books**


**Mode of Evaluation**: Continuous Assessment Test – I (CAT-I), Continuous Assessment Test – II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

**Recommended by Board of Studies** 13-12-2015

**Approved by Academic Council** No. 40 18-03-2016
<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
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<th>P</th>
<th>J</th>
<th>C</th>
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<tbody>
<tr>
<td>ECE5023</td>
<td>MEMORY DESIGN AND TESTING</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3</td>
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</tbody>
</table>

Pre-requisite: Nil

Course Objectives:
The course is aimed at:
1. Expounding the basics and detailed architecture of SRAMs and DRAMs.
2. Model the memory fault and introduce the basic and advanced memory testing patterns.
3. Elaborate the reliability and radiation effect issues of semiconductor memories and present methods for radiation hardening.
4. Review and discuss high performance memory subsystems, advanced memory technologies and contemporary issues.

Expected Course Outcome:
At the end of the course the student should be able to:
1. Design SRAMs and DRAMs.
2. Design NVRAMs and Flash Memories.
3. Model memory faults, select suitable testing patterns and develop testing patterns.
4. Incorporate DFT and BIST techniques for semiconductor memory testing.
5. Improve the reliability of semiconductor memories, simulate and model radiation effects and, perform radiation hardening.
6. Contribute to the development of high performance memory subsystems and use advanced memory technologies.

Student Learning Outcomes (SLO): 1, 6

1. Ability to apply mathematics and science in engineering applications.
6. Having an ability to design a component or a product applying all the relevant standards and with realistic constraints.

Module: 1 | Volatile memories | 5 hours
SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, SOI technology, Advanced SRAM architectures and technologies, soft error failure in SRAM, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

Module: 2 | Non-volatile memories | 5 hours
Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture.

Module: 3 | Memory Testing and Patterns | 7 hours
<table>
<thead>
<tr>
<th>Module:4</th>
<th>Design For Test and BIST</th>
<th>4 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAM Built-In Self – Test (BIST)-Weak Write Test mode – Bit Line Contact Resistance – PFET Test – Shadow Write and Shadow Read.</td>
<td></td>
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</table>

<table>
<thead>
<tr>
<th>Module:5</th>
<th>Reliability and Radiation Effects</th>
<th>7 hours</th>
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<table>
<thead>
<tr>
<th>Module:6</th>
<th>High-Performance Subsystem Memories</th>
<th>7 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories.</td>
<td></td>
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</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>Advanced Memory Technologies</th>
<th>8 hours</th>
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</thead>
<tbody>
<tr>
<td>High-Density Memory Packaging Technologies, Ferroelectric Random Access Memories (FRAMs)- Analog Memories-Magneto-resistive Random Access Memories (MRAMs)- Experimental Memory Devices Memory Hybrids and MCMs (2D)- Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability.</td>
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<td></td>
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<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2 hours</th>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Text Book(s)</th>
<th></th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Reference Books</th>
<th></th>
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| Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT). |

<table>
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<tr>
<th>Recommended by Board of Studies</th>
<th>13-12-2015</th>
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<tbody>
<tr>
<td>Approved by Academic Council No.</td>
<td>40 18-03-2016</td>
</tr>
<tr>
<td>Course Code</td>
<td>Course Title</td>
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<tr>
<td>-------------</td>
<td>-------------------</td>
</tr>
<tr>
<td>ECE5024</td>
<td>IC TECHNOLOGY</td>
</tr>
</tbody>
</table>

**Pre-requisite:** Nil

**Course Objective:**
The course is aimed to
1. Introduce the process involved in semiconductor manufacturing and fabrication.
2. Model the oxidation growth rate & to understand oxidation process and the process of diffusion and to expound the Ion Implantation process.
3. Explain the thin film deposition process and review the difference between MOS and Bipolar Process Integration.

**Expected Course Outcome:**
At the end of the course the student will be able to
1. Understand the process involved in semiconductor manufacturing and fabrication.
2. Understand the various lithography techniques used for pattern transfer.
3. Model the oxidation growth.
4. Model the diffusion mechanism in semiconductors.
5. Understand the process involved in thin film deposition.
6. Analyse the difference between MOS and Bipolar Process.

**Student Learning Outcomes (SLO):**
1, 17

1. Ability to apply mathematics and science in engineering applications.
17. Ability to use techniques, skills and modern engineering tools necessary for engineering practice.

**Module:1  | Crystal Growth | 5 hours**
Introduction to Semiconductor Manufacturing and fabrication, Clean Room types and Standards, Physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.

**Module:2  | Lithography: | 7 hours**
The Photolithographic Process, Photomask Fabrication, Comparison between positive and negative photoresists, Exposure Systems, Characteristics of Exposure Systems, E-beam Lithography, X-ray lithography.

**Module:3  | Thermal Oxidation of Silicon: | 6 hours**
The Oxidation Process, Modeling Oxidation, Masking Properties of Silicon Dioxide, Technology of Oxidation, Si-SiO2 Interface.

**Module:4  | Diffusion and Ion Implantation: | 7 hours**
<table>
<thead>
<tr>
<th>Module:5</th>
<th>Thin film deposition, contacts, packaging and yield:</th>
<th>7 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chemical Vapor Deposition, Physical Vapor Deposition, Epitaxy, Metal Interconnections and Contact Technology, Silicides and Multilayer-Contact Technology, Copper Interconnects and Damascene Processes, Wafer Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Yield.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:6</th>
<th>MOS Process Integration:</th>
<th>5 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Basic MOS Device Considerations, MOS Transistor Layout and Design Rules, Complementary MOS (CMOS) Technology.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>Bipolar Process Integration:</th>
<th>6 hours</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2 hours</th>
</tr>
</thead>
</table>

**Total Lecture hours:** 45 hours

**Text Book(s)**


**Reference Books**


**Mode of Evaluation:** Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

**Recommended by Board of Studies**

13-12-2015

**Approved by Academic Council**

No. 40 18-03-2016
<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>J</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECE5025</td>
<td>SYSTEM ON CHIP DESIGN</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

**Pre-requisite**: Nil

**Course Objective**:  
The course is aimed to  
1. Introducing design, optimization, and programing a modern System-on-a-Chip.  
2. Detailing SoC design with on-chip memories and communication networks, I/O interfacing.  
3. Making them understand about signal integrity aware SoC design and Scheduling algorithms.

**Expected Course Outcome**:  
At the end of the course the student will be able to  
1. Demonstrate an ability to identify, formulate and treat complex issues in the field of system-on-chip from a holistic perspective.  
2. Improve the performance of SoC based design by various advanced techniques.  
3. Apply SystemC for system design.  
4. Use interconnection structures in a SoC / NoC based system design.  
5. Apply static timing analysis for a SoC based design.  
6. Analyse the cause and eliminate the issues relevant to signal integrity and scheduling.

**Student Learning Outcomes (SLO):**  
1. Ability to apply mathematics and science in engineering applications.  
5. Design thinking capability.

**Module:1  Introduction**  
Architecture of the present-day SoC - Design issues of SoC- Hardware-Software Co design – Core Libraries – EDA Tools.

**Module:2  Design Methodology for Logic, Memory and Analog Cores**  

**Module:3  Introduction to System C for SoC Design**  

**Module:4  SoC and NoC Interconnection Structures**  

**Module:5  STA for SoC Design**  
Timing paths and its Timing Optimization- Slow to High and High to low frequency timing path- Half cycle timing path- Latch time borrowing- Interface Logic Model design and analysis for SoC
design.

<table>
<thead>
<tr>
<th>Module:6</th>
<th>Signal Integrity Aware SoC design</th>
<th>7 hours</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>Scheduling</th>
<th>6 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Introduction and need for HLS- Major steps-Scheduling and Allocation- Binding/Assignment- Concept of Scheduling, Heuristic Scheduling Algorithm.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2 hours</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Total Lecture hours:</th>
<th>45 hours</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Text Book(s)</th>
<th></th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Reference Books</th>
<th></th>
</tr>
</thead>
</table>

Mode of Evaluation: Continuous Assessment Test –I (CAT-I), Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

<table>
<thead>
<tr>
<th>Recommended by Board of Studies</th>
<th>13-12-2015</th>
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<tbody>
<tr>
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<td>No. 40</td>
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<td></td>
<td>18-03-2016</td>
</tr>
</tbody>
</table>
Course Code | Course Title | L | T | P | J | C
--- | --- | --- | --- | --- | --- | ---
ECE5026 | SYSTEM DESIGN WITH FPGA | 2 | 0 | 0 | 4 | 3

Prerequisite | Nil

Course Objective:
This course is aimed to
1. Review the fundamental concepts of C language.
2. Expound the architecture of NIOS II soft core processor and the various peripheral interfaces used for system design.
3. Implement the interconnect fabrics for the system and to design the system using NIOS II Soft core Processor.

Expected Course Outcome:
After completion of the course the student will be able to:
1. Understand the concepts of C language.
2. Understand the NIOS II soft core processor architecture.
3. Interpret the usage of various peripheral interfaces for system design.
4. Develop system by choosing suitable interconnect fabrics.
5. Design the system using NIOS II soft core processor.
6. Model the system by using IP block.
7. Design and develop embedded synthesis using FPGA.

Student Learning Outcomes (SLO): 5, 12, 17
- 5. Having design thinking capability
- 12. Having adaptive thinking and adaptability
- 17. Having an ability to use techniques, skills and modern engineering tools necessary for engineering practice.

Module: 1 | Basic C Concepts | 5 hours
--- | --- | ---
Loops, Arrays, structures, pointers, functions, linked list

Module: 2 | Soft Core Processor | 5 hours
--- | --- | ---
Nios II Processor – Configurability Features – Processor Architecture-Instruction set

Module: 3 | Peripheral Interfaces | 5 hours
--- | --- | ---
LCD, PS2, RS232, SDRAM, SRAM Controller, VGA, Audio and Video, PIO, External Bus bridge and IrDA

Module: 4 | NIOS II programming for peripheral Interfaces | 4 hours
--- | --- | ---
LCD, PS2, RS232, SDRAM, SRAM, VGA, Audio, IrDA.

Module: 5 | Interconnect Fabrics | 3 hours
--- | --- | ---
Avalon Switch Fabric Interconnect - Implementation and Functions- Integrated Design Environment

Module: 6 | System Design | 4 hours
--- | --- | ---
Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, LCD, Camera
<table>
<thead>
<tr>
<th>Module:7</th>
<th>IP Block Implementation</th>
<th>2 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Edge detection algorithm, Colour and Brightness Enhancement algorithm</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2 hours</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Total Lecture hours:</th>
<th>30 hours</th>
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</thead>
</table>

**Text Book(s)**


**Reference Books**


Mode of Evaluation: Continuous Assessment Test –I (CAT-I), Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

**Typical Projects**

1. Implementation of edge detection algorithm
2. Implementation of self-guided vehicle.
3. Implementation of smart home system
4. Implementation of Health Monitoring System
5. Implementation of Music Synthesizer.

Mode of Evaluation: Review I, II and III

<table>
<thead>
<tr>
<th>Recommended by Board of Studies</th>
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<tr>
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</table>

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Approved by Academic Council No. 40 18-03-2016
<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
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<th>P</th>
<th>J</th>
<th>C</th>
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</thead>
<tbody>
<tr>
<td>ECE5027</td>
<td>ADVANCED COMPUTER ARCHITECTURE</td>
<td>3</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

Pre-requisite: Nil

Course Objective:
The course is aimed to
1. Introduce advanced concepts of computer architecture.
2. Acquire knowledge on various interconnect topology for multiprocessor system and different pipelining techniques.
3. Understanding different memory hierarchy for multiprocessor and multicomputer systems.

Expected Course Outcomes:
At the end of the course the student will be able to:
1. Understand the architecture of the various multiprocessors and multicomputer.
2. Identify possible parallel execution at hardware and software level.
3. Design required static or dynamic interconnect network for a multiprocessor system.
4. Apply different pipelining techniques to reduce computation time.
5. Analyse the various memory design for multiprocessor and multicomputer.
6. Design scalable parallel architecture for multiprocessor system.

Student Learning Outcomes (SLO): 1, 5
1. Ability to apply mathematics and science in engineering applications
5. Design thinking capability

Module: 1 Parallel computer models 3 hours
- The state of computing - Classification of parallel computers - Multiprocessors and Multicomputer - Multivector and SIMD computers.

Module: 2 Program and network properties 7 hours
- Conditions of parallelism - Data and resource Dependences - Hardware and software parallelism - Program partitioning and scheduling - Grain Size and latency - Program flow mechanisms - Control flow vs data flow - Data flow Architectures.

Module: 3 System Interconnect Architectures 7 hours
- Network properties and routing - Static interconnection Networks - Dynamic interconnection Networks - Multiprocessor system Interconnects - Hierarchical bus systems - Crossbar switch and multiport memory - Multistage and combining network.

Module: 4 Pipelining 7 hours
- Linear pipeline processor - nonlinear pipeline processor - Instruction pipeline Design - Mechanisms for instruction pipelining - Dynamic instruction scheduling - Branch Handling techniques - branch prediction - Arithmetic Pipeline Design

Module: 5 Memory Hierarchy Design 6 hours
- Cache basics & cache performance - reducing miss rate and miss penalty - multilevel cache hierarchies - main memory organizations - design of memory hierarchies.

Module: 6 Shared Memory Architectures 7 hours
- Symmetric shared memory architectures - distributed shared memory architectures - cache
coherence protocols - scalable cache coherence - directory protocols - memory based directory protocols - cache based directory protocols.

<table>
<thead>
<tr>
<th>Module:7</th>
<th>Multiprocessor Architectures</th>
<th>6 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Computational models - An Argument for parallel Architectures - Scalability of Parallel Architectures - Benchmark Performances.</td>
<td></td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2 hours</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Total Lecture hours:</th>
<th>45 hours</th>
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**Text Book(s)**


**Reference Books**


**Mode of Evaluation:** Continuous Assessment Test – I (CAT-I), Continuous Assessment Test – II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

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<td>No. 40</td>
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</table>

1. Approved by Academic Council No. 40 18-03-2016
Course Code | Course Title                              | L | T | P | J | C  
---|---|---|---|---|---|---
ECE5028 | MICROSENSORS AND INTERFACE ELECTRONICS   | 2 | 0 | 0 | 4 | 3  
Pre-requisite | Nil  

Course Objective:
The course is aimed to
1. Introduce various types of Microsensors & micro actuators corresponding materials to fabricate it.
2. Make them understand the concepts of Microsystem technologies used for realizing Microsensors and actuators.
3. Explore the working principles of interface electronics circuits for resistive, capacitive and temperature sensors.

Expected Course Outcome:
After the completion of the course, students will be able to:
1. Understand the Micro and Smart Systems.
2. Identify MEMS materials and Properties.
3. Understand the fabrication process flow for Microsystems.
4. Classify and Comprehend different types of Sensors and Actuators.
5. Explain about the wide applications of Microsensors.
6. Understand the basic Interface Circuits.
7. Understand the approach in design of Sensor Interface circuits.

Student Learning Outcomes (SLO): 1, 6, 14
1. Ability to apply mathematics and science in engineering applications
6. Ability to design a component or a product applying all the relevant standards and with realistic constraints
14. Ability to design and conduct experiments, as well as to analyze and interpret data.

Module: 1  Introduction to Micro and Smart Systems  3 hours
Microsystems and scaling law, MEMS & Micro machines, Evolution of Microsystems, Silicon and Non-silicon Micro and Smart Systems, Market for Microsystems.

Module: 2  Microsystem Materials and Properties  3 hours
Materials - Silicon, Silicon oxide and nitride, Thin Metal films (Cr, Au, Ti, Pt), Polymers (SU8, PMMA, PDMS), Glass and Quartz.
Important material properties - Young modulus, Poisson’s ratio, density, piezoresistive coefficients, TCR, Thermal Conductivity, Material Structure.

Module: 3  Micro System Technology  5 hours

Module: 4  Introduction to Sensors and Actuators  4 hours
Electrostatic, Piezoelectric, Piezoresistive, Electromagnetic, Thermo pneumatic, Shape Memory Alloy, Thermoelectric, Optical and Resonant.
Module:5 | Applications of Micro Devices | 4 hours
---|---|---
Telecommunication Applications: Imaging and Displays, Fiber optic communication devices.

Module:6 | Interface Circuits | 5 hours
---|---|---
Interface circuits for Resistive, Capacitive and Temperature Sensors

Module:7 | Voltage and Current - Mode Approach in Sensor Interfaces Design | 4 hours
---|---|---
Voltage-Mode Approach in Sensor Interfaces Design, DC & AC excitation for resistive sensors, capacitive sensor interfacing, temperature sensor interfaces.

Module:8 | Contemporary issues: | 2 hours
---|---|---

Text Book(s)

Reference Books

Mode of Evaluation: Continuous Assessment Test –I (CAT-I), Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

List of Projects (Indicative)
1. Design of Piezoelectric cantilever for energy harvesting applications.
2. Fault detection using accelerometer and gyroscope.
3. Design of Silicon pressure sensors for car tire pressure monitoring.
4. PDMS pressure sensor for disposable blood pressure sensors.
5. PDMS grippers for the micromanipulation of biological cells.
6. Thermoactuator switches for optical signal control.
7. Design of Gas sensors for automobiles.

Mode of Evaluation: Review I, II & III

Recommended by Board of Studies | 13-12-2015
Approved by Academic Council | No. 40 | 18-03-2016
Course Code | Course Title | L | T | P | J | C
--- | --- | --- | --- | --- | --- | ---
ECE5029 | VLSI TESTING AND TESTABILITY | 3 | 0 | 0 | 0 | 3

Pre-requisite: Nil

**Course Objective:**

The course is aimed to
1. Model and simulate different types of faults in digital circuits at the gate level.
2. Establish equivalence and dominance relationships of faults in a circuit.
3. Compare automatic test pattern generation algorithms with respect to search space, speed, fault coverage and other criteria.
4. Handle design complexity, ensure reliable operation, and achieve short time-to-market using various testing methodologies.

**Expected Course Outcome:**

After completion of the course students will be able to:

1. Model different fault models.
2. Simulate faults and generate test patterns for combinational circuits.
3. Apply scan based testing.
4. Recognize the BIST techniques for improving testability.
5. Understand boundary scan based test architectures.
6. Analyse and apply the test vector compression techniques for memory reduction and fault diagnosis.

**Student Learning Outcomes (SLO):** 1,17

1. Ability to apply mathematics and science in engineering applications.
17. Ability to use techniques, skills and modern engineering tools necessary for engineering practice.

**Module:1  Fault Modelling**

6hours

**Module:2  Fault Simulation and Test Generation**

7hours
Fault Simulation: Serial, Parallel, Deductive, Concurrent - Combinational Test Generations - ATPG for Combinational Circuits - D-Algorithm - Testability Analysis - SCOAP measures for Combinational Circuits

**Module:3  Scan based Testing**

7hours

**Module:4  Built-in Self-Test**

7hours
<table>
<thead>
<tr>
<th>Module:5</th>
<th>Boundary scan and Core based Testing</th>
<th>5hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Digital Boundary Scan (IEEE Std. 1149.1): Test Architecture and Operations - On-Chip Test Support with Boundary Scan - Board and System-Level Boundary-Scan Control Architectures.</td>
<td></td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Module:6</th>
<th>Test Compression and Compaction</th>
<th>6hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Test Stimulus Compression: Code-Based Schemes, Linear-Decompression-Based Schemes - Test Response Compaction.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>Fault Diagnosis</th>
<th>5hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Dictionary Based and Adaptive fault diagnosis.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Total Lecture hours:</td>
<td>45hours</td>
</tr>
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</table>

<table>
<thead>
<tr>
<th>Text Book(s)</th>
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</table>

Mode of Evaluation: Continuous Assessment Test –I (CAT-I), Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Recommended by Board of Studies 13-12-2015
Approved by Academic Council No. 40 18-03-2016
Course code | Scripting languages for VLSI design automation | L T P J C
--- | --- | ---
ECE 5030 | 2 0 2 0 3
Pre-requisite | None | Syllabus version
--- | --- | ---
--- | --- | ---

Course Objectives:
The course is aimed to
1. To write scripts in the LINUX environment.
2. To study the principles of Scripting Languages like Perl, TCL and Python.
3. To write the scripts for automation using the languages like Perl, TCL and Python.

Expected Course Outcome:
At the end of the course the students will be able to
1. Work in LINUX environment.
2. Develop the PERL scripts
3. Develop the TCL & TK scripts for automation
4. Develop the python scripts for automation
5. Write scripts for a given EDA design automation

Student Learning Outcomes (SLO): 1,14,17
1. Having an ability to apply mathematics and science in engineering applications
14. Having an ability to design and conduct experiments, as well as to analyze and interpret data
17. Having an ability to use techniques, skills and modern engineering tools necessary for engineering practice.

Module:1 LINUX Basics | 3 hours
--- | ---
Introduction to Linux, File System of Linux, General usage of Linux Kernel and Basic Commands, Linux users and group, Permissions for file, directory and users, Searching a file and directory, zipping and unzipping concepts.

Module:2 PERL Basics | 5 hours
History and Concepts of PERL - Scalar Data - Arrays and List Data - Control structures – Hashes - Basics I/O - Regular Expressions – Functions - Miscellaneous control structures - Formats.

Module:3 Advanced Topics in PERL | 4 hours

Module:4 TCL Basics | 4 hours

Module:5 Advanced Topics in TCL | 4 hours

Module:6 Python Basics | 4 hours
Introduction to Python – Using Python interpreter – Control flow Tools – Data structures – Modules

Module:7 Advanced Topics in Python | 4 hours
Input and Output – Errors and Exceptions – Classes – Brief tour on standard library
### Module: 8

**Contemporary issues:**

| Total Lecture hours: | 30 hours |

### Reference Books


### Mode of Evaluation: CAT / Assignment / Quiz / FAT / Project / Seminar

### List of Challenging Experiments (Indicative)

<table>
<thead>
<tr>
<th>Experiment Description</th>
<th>Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Write a script to generate random test vectors for a given Verilog design.</td>
<td>3</td>
</tr>
<tr>
<td>2. Write a script which reads a verilog design module and identifies whether it is a sequential or combinational design. Accordingly, the perl script should generate the testbench file in verilog. Also, the input vectors from the testbench should be in a randomized fashion.</td>
<td>3</td>
</tr>
<tr>
<td>3. Write a script that reads a set of log files from different simulation directories and generates a consolidated report in .xls format which should contain the information of the test name, status and error messages. If the test is indicated as successful in the log file, the status in the report should be as “TEST PASSED” and if the test is unsuccessful, then the report should display the status as “TEST FAILED”.</td>
<td>2</td>
</tr>
<tr>
<td>4. Write a TCL Script which when executed should automatically compile your design modules and testbench modules and then perform the simulation. If the simulation is successful, then the script should synthesize the design module. The TCL script should also create a separate directory to dump the log files and a separate directory to write the netlist file.</td>
<td>3</td>
</tr>
<tr>
<td>5. Write a script to perform netlist patching.</td>
<td>2</td>
</tr>
<tr>
<td>6. Verification automation tool development using Perl/Python scripts</td>
<td>2</td>
</tr>
</tbody>
</table>

**Total Laboratory Hours**

| Total Laboratory Hours | 15 hours |

**Mode of evaluation:** Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

**Recommended by Board of Studies**

| Date | 05-03-2019 |

**Approved by Academic Council**

| No. | 54 |

| Date | 14-03-2019 |
Course code: VLSI Verification Methodologies
ECE 6024
Pre-requisite: ECE5017 Digital Design with FPGA

Course Objective:
1. To introduce various verification techniques.
2. To write Testbench using System Verilog.
3. To develop UVM test bench environment

Expected Course Outcome:
The students will be able to:
1. Comprehend the VLSI verification techniques.
2. Define classes and create objects.
3. Develop design using system verilog.
5. Cognize the UVM Verification environment.
6. Create reusable verification environment using UVM.

Student Learning Outcomes (SLO): 1, 14, 17
1. Having an ability to apply mathematics and science in engineering applications
14. Having an ability to design and conduct experiments, as well as to analyze and interpret data
17. Having an ability to use techniques, skills and modern engineering tools necessary for engineering practice.

Module: 1 Verification Techniques 4 hours

Module: 2 Basic OOP 3 hours
OOP Terminology, Creating Object, object deallocation, copying objects, static variables, Global variables, Inheritance, Polymorphism

Module: 3 System Verilog – Data Types & Procedural statements 6 hours

Module: 4 Connecting Testbench and Design 3 hours
Program, Interface, Stimulus timing, Module interactions, Connecting together, Development of self-checking test environment – Generator, Transactor, Driver, Monitor, Checker, Scoreboard

Module: 5 Randomization, Assertion and Coverage 3 hours
Randomization in system Verilog, Constraints, Functional coverage, cross coverage, cover groups, Assertions

Module: 6 Universal Verification Methodology 4 hours
Introduction to UVM - Verification components - Transaction level modeling

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<thead>
<tr>
<th>Module:7</th>
<th>UVM – Verification Environments</th>
<th>5 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Developing reusable verification components - Using Verification components – Developing reusable verification environment – Register classes.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Total Lecture hours:</th>
<th>30 hours</th>
</tr>
</thead>
</table>

Reference Books:


Mode of Evaluation:

- CAT / Assignment / Quiz / FAT / Project / Seminar

List of Challenging Projects (Indicative)

1. Develop a system Verilog testbench to verify your DUT by following the steps given below.
   i) Write the following blocks in system Verilog to verify your design
      a. Program Block
      b. Interface Block with clocking block and modport
      c. Top Level Harness file which has the instance of your DUT, test program and the interface.
   ii) Develop the Generator, Transactor and Driver components for your DUT
   iii) Develop the self-checking feature by writing the receiver, monitor and checker components for your DUT.
   iv) Simulate and verify the output.

2. Define a packet class to encapsulate the packet information and create random packet objects in the generator then send, receive and check the correctness of the DUT using the packet objects for the given router IP. Follow the instructions given in the lab to complete the task. Simulate and verify the output for the good RTL code and the faulty code. Include covergroups and check the functional coverage is greater than 90%.

Mode of evaluation: Continuous Assessment Test –I (CAT-I), Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

Recommended by Board Of Studies 05-03-2019
Approved by Academic Council No. 54 Date 14-03-2019
<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course title</th>
<th>L</th>
<th>T</th>
<th>P</th>
<th>J</th>
<th>C</th>
</tr>
</thead>
<tbody>
<tr>
<td>ECE6025</td>
<td>LOW POWER IC DESIGN</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>Pre-requisite</td>
<td>ECE5015 - Digital IC Design</td>
<td></td>
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</tbody>
</table>

**Course Objective:**

The course is aimed to

1. Understand the concepts and techniques of Low power VLSI.
2. Develop a broad insight into the methods used to confront the low power issue from lower level (circuit level) to higher levels (system level) of abstraction.
3. Develop a system with multiple supply and threshold voltages used for low power DSP applications.

**Expected Course Outcome:**

After completion of the course student will be able to:

1. Understand the factors affecting the power in VLSI circuits.
2. Apply algorithmic and architectural level power optimization methods.
3. Apply logic and circuit level power optimization techniques.
4. Apply register transfer level power optimization techniques.
5. Develop an optimum code to reduce the power in the software level.
6. Analyse and explore the usage of sleep transistors for low power.
7. Develop power efficient IPs.

**Student Learning Outcomes (SLO):**

1, 5, 9, 17

2. Having a clear understanding of the subject related concepts and of contemporary issues.
5. Having design thinking capability.
17. Ability to use techniques, skills and modern engineering tools necessary for engineering practice.

**Module:1 Introduction to Low Power Design Methods**

3 hours

Motivation- Context and Objectives- Sources of Power dissipation in Ultra Deep Submicron CMOS Circuits – Static, Dynamic and Short circuit components Effects of scaling on power consumption- Low power design flow- Normalized Figure of Merit – PDP& EDP- Overview of power optimization at various levels.

**Module:2 Algorithmic and Architecture Level Optimization**

5 hours

Pipelining and Parallel Processing approaches for low power in DSP filter structures- Multiple supply voltage and Multiple threshold voltage designs for low power- Computer arithmetic techniques for low power- Optimal drivers of high speed low power- software level power optimization.

**Module:3 Logic Level and Circuit Level Optimization**

5 hours

Theoretical background – Calculation of Steady state probability- Transition probability - Conditional probability- Transition density- Estimation and optimization of Switching activity-Power cost computation model.

Transistor variable re-ordering for power reduction- Low power library cell design (GDI)- Estimation of glitching power- leakage power optimization-Subthreshold logic design.
<table>
<thead>
<tr>
<th>Module:4</th>
<th>Register Transfer Level Optimization</th>
<th>4 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low power clock-Interconnect and layout designs- Low power memory design and low power SRAM architectures- Clock gating- Bus Encoding techniques-Deglitching for low power.</td>
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</table>

<table>
<thead>
<tr>
<th>Module:5</th>
<th>Low Power Design of Sub-Modules</th>
<th>5 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Circuit techniques for reducing power consumption in Adders- Multipliers. Synthesis of FSM for low power- Retiming sequential circuits for low power.</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:6</th>
<th>Sleep Transistor Design</th>
<th>3 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Design metrics- switch efficiency- area efficiency- IR drop, normal Vs reverse body bias -Layout design of Area efficiency- Single row Vs double row- Inrush current and current latency.</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:7</th>
<th>IP Design for Low Power</th>
<th>3 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Architecture and partitioning for power gating- power controller design for the USB OTG- Issues in designing portable power controllers- clocks and resets- Packaging IP for reuse with power intent.</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues:</th>
<th>2 hours</th>
</tr>
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<tbody>
<tr>
<td>Total Lecture hours:</td>
<td>30 hours</td>
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<table>
<thead>
<tr>
<th>Text Book(s)</th>
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<table>
<thead>
<tr>
<th>Reference Books</th>
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</thead>
</table>

| Mode of Evaluation:Continuous Assessment Test –I (CAT-I), Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT). |

<table>
<thead>
<tr>
<th>List of Projects (Indicative)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Design of Low Power, High Speed VLSI Adder and Multiplier Subsystems</td>
</tr>
<tr>
<td>2. Power Gating Design solutions for Low Power</td>
</tr>
<tr>
<td>3. Circuit level power reduction using multi-V_t</td>
</tr>
<tr>
<td>4. Non-conventional Low Power Circuits such as Energy Recovery Logic</td>
</tr>
<tr>
<td>5. Design of Low Power Clocking Solution for a Sequential System</td>
</tr>
<tr>
<td>6. Low power SRAM and CAM design</td>
</tr>
<tr>
<td>7. Low Power FFT Design for Wireless Communication Systems</td>
</tr>
<tr>
<td>8. Low Power Filter design for SDR systems.</td>
</tr>
</tbody>
</table>

Mode of Evaluation: Review I, II & III
Recommended by Board of Studies 13-12-2015
Approved by Academic Council No. 40 18-03-2016
<table>
<thead>
<tr>
<th>Course Code</th>
<th>Course Title</th>
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<tbody>
<tr>
<td>ECE6026</td>
<td>MIXED SIGNAL IC DESIGN</td>
<td>2</td>
<td>0</td>
<td>0</td>
<td>4</td>
<td>3</td>
</tr>
</tbody>
</table>

Pre-requisite: ECE5016-Analog IC Design

Course Objective:
The course is aimed to
1. introduce the design aspects of dynamic analog circuits and analog-digital interface electronics in CMOS technology.
2. Specify design implement ADC & DAC.

Expected Course Outcome:
At the end of the course the student will be able to
1. Understand the theory of discrete-time signal processing and its implementation using analog techniques.
2. Realizing Sample and Hold Circuits using MOS by considering the non-idealities.
3. Analyse CMOS based Switched Capacitor Circuits.
4. Understanding basics of Data Converters.
5. Analyse the architectures of ADCs and DAC.
6. Understand the oversampling converter architecture.
7. Gain mixed-signal design experience using Cadence EDA tools.

Student Learning Outcomes (SLO): 1,5,17
Student Learning Outcomes involved:
1. Ability to apply mathematics and science in engineering applications aving a clear understanding of the subject related concepts and of contemporary issues
5. Having design thinking capability
17. Having an ability to use techniques, skills and modern engineering tools necessary for engineering practice.

Module:1 | Sampling | 3 hours

Module:2 | Sampling Circuits: | 3 hours
Sampling circuits- Distortion due to switch - Charge injection - Thermal noise in sample and holds - Bottom plate sampling - Gate bootstrapped switch -Nakagome charge pump. Characterizing Sample and hold - Choice of input frequency.

Module:3 | Switched Capacitor Circuits: | 4 hours

Module:4 | A/D and D/A Converters Fundamentals: | 2 hours

Module:5 | Analog to Digital Converter Architectures: | 4 hours
Flash ADC - Regenerative latch - Preamp offset correction - Preamp Design - necessity of up-front sample and hold for good dynamic performance. Folding ADC - Multiple-Bit Pipeline ADCs and SAR ADC.

**Module:6 Digital to Analog Converter Architectures:** 5hours

- DAC spectra and pulse shapes - NRZ vs RZ DACs. DAC Architectures: Binary weighted - Thermometer DAC - Current steering DAC - Current cell design in current steering DAC - ChargeScaling DAC - Pipeline DAC.

**Module:7 Oversampling Converter:** 7hours


**Module:8 Contemporary issues:** 2hours

<table>
<thead>
<tr>
<th>Text Book(s)</th>
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</thead>
</table>

**Reference Books**


Mode of Evaluation: Continuous Assessment Test –I (CAT-I), Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

**Typical Projects**

1. Design of Flash ADC
2. Design of High Speed Sample and Hold Amplifier.
3. Design of Charge Pump Circuit.
4. Design of Switched Capacitor Integrator
5. Design of Current – Steering DAC

Mode of Evaluation: Review I, II & III

**Recommended by Board of Studies**

| 13-12-2015 |
| Approved by Academic Council |

| No. 40 |

| 18-03-2016 |
Course Code: ECE6027  
Course Title: RFIC DESIGN  
L | T | P | J | C  
---|---|---|---|---  
2 | 0 | 0 | 4 | 3  

Pre-requisite: ECE5016 - Analog IC Design

Course Objectives:  
The course is aimed at  
1. To become familiarize with the design of integrated radio front-end circuits.

Expected Course Outcomes:  
At the end of the course the student should be able to  
1. Understand the concepts of RF IC Design.  
2. Understand the High Frequency model of MOS and importance of Impedance Matching.  
3. Analyse the various transceiver and radio architectures.  
5. Realize VCOs and Frequency synthesizers and their applications to transceiver design.  
6. Classify and comprehend the design of Power Amplifiers.  
7. Gain RFIC design experience in Cadence CAD tools.

Student Learning Outcomes (SLO): 5,17
Student Learning Outcomes involved:  
5. Having design thinking capability  
17. Having an ability to use techniques, skills and modern engineering tools necessary for engineering practice.

Module:1  
Introduction to RF & Wireless Technology: 5hours  

Module:2  
High Frequency Model of RF Transistors and Matching Networks: 4hours  
MOSFET behaviour at RF frequencies - Noise performance and limitation of devices - Impedance matching networks - transformers and baluns.

Module:3  
Analog& Digital Modulation for RF Circuits: 4hours  

Module:4  
Low Noise Amplifiers and Mixers 4hours  
Low Noise Amplifiers: Common Source LNA - Common Gate LNA -Cascode LNA. Mixers: Design of Active and Passive Mixers.

Module:5  
Voltage Controlled Oscillators and Frequency Synthesizers: 3hours  
Synthesizers: PLLs.

**Module:6**  **RF Power Amplifiers:** 4hours
Class A, AB, B, C amplifiers - Class D, E, F amplifiers - RF Power amplifier design.

**Module:7**  **Radio architectures:** 4hours
GSM radio architectures, CDMA, UMTS radio architectures.

**Module:8**  **Contemporary issues:** 2hours

| Total Lecture hours: | 30hours |

**Text Book(s)**

**Reference Books**

**Mode of Evaluation:** Continuous Assessment Test – I (CAT-I), Continuous Assessment Test – II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / Innovative ideas leading to solutions for industrial problems, Final Assessment Test (FAT).

**List of Projects (Indicative)**
1. I-V Characterisation study of RF device/circuit
2. Design of Low Noise Amplifier
3. Design of Voltage Controlled Oscillators
4. Design of Power Amplifiers
5. Design and Implement- any one of the Receiver architecture

**Mode of Evaluation:** Review I, II & III

<table>
<thead>
<tr>
<th>Recommended by Board of Studies</th>
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<tbody>
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<td>No. 40</td>
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<tr>
<td></td>
<td>18-03-2016</td>
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</tbody>
</table>
### Course Objective:

The course is aimed to

1. Make student to understand CMOS scaling
2. understand theory and operation of multigate MOSFET and analog design digital, circuits using multigate devices materials and their properties used for designing Microsensors.
3. understand the concepts of Microsystem technologies used for realizing Microsensors and actuators.
4. understand the working principles of Interface Electronic Circuits for resistive, capacitive and temperature sensors.

### Expected Course Outcome:

At the end of the course the students will be able to

1. Understand the CMOS scaling
2. explain the need of novel MOSFET.
3. explain the physics of multigate MOS system
4. model nanowire FETs.
5. Design digital and analog circuit using multigate devices.
6. Understand the physics of CNTFET
7. Develop analytical model for novel FETs and validate them by numerical simulations.

### Student Learning Outcomes (SLO):

- Design thinking capability.
- Ability to use techniques, skills and modern engineering tools necessary for engineering practice.

<table>
<thead>
<tr>
<th>Module:1</th>
<th>CMOS Scaling Issues and Solutions</th>
<th>2hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MOSFET scaling, short channel effects, quantum effects, volume inversion, threshold voltage, channel engineering, source/drain engineering, high-k dielectric, strain engineering, multigate technology mobility, gate stack.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:2</th>
<th>Introduction to Novel MOSFETs</th>
<th>2hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SOI MOSFET, multigate transistors, single gate, double gate, triple gate, surround gate, Silicon Nanowire transistors</td>
<td></td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:3</th>
<th>Physics of Multi-gate MOS System</th>
<th>5hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>MOS electrostatics, 1D, 2D MOS electrostatics, ultimate limits, double gate MOS system, gate voltage effect, semiconductor thickness effect, asymmetry effect, oxide thickness effect, electron tunnel current, two dimensional confinement, scattering</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:4</th>
<th>Nanowire FETS</th>
<th>5hours</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Silicon nanowire MOSFETs, evaluation of I-V characteristics, I-V characteristics for non-degenerate carrier statistics, I-V characteristics for degenerate carrier statistics, electronic conduction in molecules, general model for ballistic nano transistors, CNT-FETs</td>
<td></td>
</tr>
<tr>
<td>Module:5</td>
<td>Digital Circuit Design using Multi-gate Devices</td>
<td>5 hours</td>
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</tr>
<tr>
<td>Digital circuits design, impact of device performance on digital circuits, leakage performance trade off, multi VT devices and circuits, SRAM design</td>
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</table>

<table>
<thead>
<tr>
<th>Module:6</th>
<th>Analog Circuit Design using Multi-gate Devices</th>
<th>5 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog circuit design, trans-conductance, intrinsic gain, flicker noise, self-heating, band gap voltage reference, operational amplifier, comparator designs, mixed signal, successive approximation DAC, RF circuits</td>
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</tbody>
</table>

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<thead>
<tr>
<th>Module:7</th>
<th>Carbon Nanotube FET</th>
<th>4 hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT-FET, CNT memories, CNT based switches, logic gates, CNT based RF devices, CNT based RTDs, CNTFET based applications</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Module:8</th>
<th>Contemporary issues</th>
<th>2 hours</th>
</tr>
</thead>
</table>

| Total Lecture hours: | 30 hours |

**Text Book(s)**

**Reference Books**

Mode of Evaluation:Continuous Assessment Test –I (CAT-I) , Continuous Assessment Test –II (CAT-II), Seminar / Challenging Assignments / Completion of MOOC / QUIZ, Final Assessment Test (FAT).

**List of Projects**
1. Design and Extraction of DC and AC parameters of MOSFET with Source/Drain Extension
2. Performance Analysis of Double/Triple/Surround gate devices
3. Analysis of Gate Work Function Engineering in Multi-gate Devices
4. Single Event Upset/Soft Error Analysis in Multi-gate FETs
5. Comparison of CMOS and Fin FET based SRAM
6. Design of OTA and Comparator in Multi-gate Devices

Mode of Evaluation:Review I, II & III

**Recommended by Board of Studies** 13-12-2015
**Approved by Academic Council** No. 40 18-03-2016