VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Three Days Hands- on workshop

On

Digital IC Design using Cadence Tools

Department of Micro and Nanoelectronics
School of Electronics Engineering

About the Course: The value added course on Analog and Digital VLSI Design Logic to Layout, aim to introduce the most demand skills in VLSI. This course deals with the fundamental theory to Practical hand on training in vlsi. This course allows the student to learn from the scratch to write code , design using the CMOS transistors which help them to manage their projects efficiently and make the career as a vlsi design engineer.

From 12-05-2023 to 14-05-2023

Highlight of the Course:

- Introduction to Verilog & CMOS
- Practical training: How to write code using Verilog HDL Programming.
- Practical training: How to design Semicustom Digital VLSI circuits using Cadence tools.
- Mini Project based on lower node
- E Certificate

Course Experts

Industry: Mr. Suprovab Mandal, Lead Engineer, Microchip. Malaysia

Faculty: Dr. Ravi S. SENSE

Dr. Satheesh kumar . SENSE

Dr.Rajeev Pankaj, SENSE

Alumni: Alumni Industry Engineers

Advisory Committee

Dr. Sivanantham S, Professor & Dean, School of Electronics Engineering

Dr. Jagannadha Naidu,

HOD- Dept of Micro and Nanoelectronics, SENSE

Faculty Coordinators:

Dr. S Ravi, SENSE
Email: msravi@vit.ac.in

Dr. Satheeshkumar S , SENSE,

satheeshkumar.s@vit.ac.in

Dr.Rajeev Pankaj Nelapaty,SENSE

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Target Audience: UG/PG students & Research Scholars

- **Registration Fee:** Rs 1770. **Payment Link:** https://events.vit.ac.in/

Seats Limited to 50 Participants

Contact Numbers
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