School of Electronics Engineering

Department of Embedded Technology

VIVADO™

Value Added Course

DIGITAL SYSTEM DESIGN WITH FPGA(VAC1986)- Verilog & VHDL

Day 1 (23/03/24) 9:00 AM to 1:00 PM

- Modelling Half-adder, Half-Subtractor, Full adder and Full Subtractor in Vivado Design Suite

Day 2 (24/03/24) 9:00 AM to 1:00 PM

- Modelling Multiplexer and Demultiplexer in Vivado Design Suite

Day 3 (08/04/24) 5:00 PM to 7:00 PM

- Modelling Decoder and Encoder in Vivado Design Suite

Day 4 (09/04/24) 5:00 PM to 7:00 PM

- Modelling Arithmetic and Logic Unit in Vivado Design Suite

Day 5 (10/04/24) 5:00 PM to 7:00 PM

- Modelling of Flip Flops in Vivado Design Suite

Day 6 (11/04/24) 5:00 PM to 7:00 PM

- Modelling of different types of counters in Vivado Design Suite

Day 7 (12/04/24) 5:00 AM to 7:00 PM

- Finite State Machine based sequence Detector in Vivado Design Suite

Day 8 (13/04/24) 9:00 AM to 1:00 PM

- Modelling of real time systems on an FPGA

Day 9 (15/04/24) 5:00 PM to 7:00 PM

- Modelling of waveform generator using FPGA.

Day 10 (16/04/24) 5:00 PM to 7:00 PM

- Working with LEDs and Switches.

Day 11 (17/04/24) 5:00 PM to 7:00 PM

- Working with LCD Display.

Day 12 (18/04/24) 5:00 PM to 7:00 PM

- Modelling complete 8-bit microcontroller on an FPGA.

Interaction ONLINE : MS Team & OFFLINE: TT 603

Eligibility: B. Tech and M.Tech Students who are all interested to learn Verilog and VHDL

Starting from

23rd March, 2024 (Saturday)

Registration fee: Rs. 250/- + GST

Registration Link: https://events.vit.ac.in/

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9786026007

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