VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Two-week National level Workshop on

System On Chip Design Using OpenPOWER

20th November to 2nd December 2023

(Online)

Organized by
School of Electronics Engineering

VENUE: TT727
Technology Tower
Vellore Institute of Technology,
Vellore-632 014.
India.

Why Open Source - Hardware?

1. This is a multi-faceted challenge and many parts need to fall into place for a fully open design.

2. Open-Source architectures and interconnect standards RISC V and OpenPOWER are relatively recent (license free). Additions, with OpenPOWER being a high level architecture. That is and license free for architecture compliant designs.

Benefits to the participants

To understand

i. OpenPOWER processor architectures and OpenPOWER based SoC development. Design of OpenPOWER based SoCs in hardware, description language. Low-level software design for OpenPOWER based SoCs and high-level application development.

ii. Ability to evaluate implementation results (e.g. speed, area, power) and correlate them with the corresponding high level design and capture.

iii. Ability to use tools to develop OpenPOWER based SoCs. EDA Tools as well as PDK tools experience.

Time: 10:00 AM to 04:00 PM (IST)

Mode: Hybrid mode
(Both online and offline)
For further informations visit us at:
www.vit.ac.in

About the Event

The workshop has been designed to impart programming knowledge and skills required for being an effective researcher/teacher within the domain of IBM FPGAs based design. The workshop is open to faculty, persons from industry, doctoral and other students. This workshop will have specific sessions which include sessions on Chip design & verification using IBM Open Core; instruction set architecture, FPGA implementation, open source LibreSoC etc.. The programme will give opportunities to connect with experts for research orientation.

Who can attend?

- Faculty Members Research
- Scholars Industry Professionals
- PG Students / UG Students*

* Pre-requisite:
Basic knowledge on digital system design

Registration Fees:

Academicians (Faculty/Scholars/Students)	Rs.2000 + GST
Industry Professionals	Rs.3000 +GST

*There is no registration fee for VIT Vellore internal faculty only. Separate forms will be circulated for registration process.

Registration/Payment Link:

https://events.vit.ac.in/
Extended Date for Registration:
18th November 2023

IBM OpenPOWER OBJECT AUTOMATION AI Hardware and Software Solutions

Topics

Course Contents:

- *OpenPOWER Core and Accelerators*
- *POWER ISA features*
- *Softcore for FPGA- Microwatt Introduction*
- *System on a chip and Components*
- *System Verilog*
- *Chiplet and OpenPOWER Cores*
- *Power Architecture Curriculum Summary*
- *FPGA Implementation*
- *Libre SOC features*
- *Verification Concepts*
- *Components of Verification and Examples*
- *Programming, Coriolis2 Flow for GDS II.*

For Quarries contact: **Dr. Sateesh Kumar .S,**
8124424714

Applications will be accepted on a first come first serve basis. The number of participants is limited to 100 numbers. Selected participants will receive online link to attend the Sessions.

80 HOURS COURSE

OREGON

BroadPak
2.5D/3D Technologies
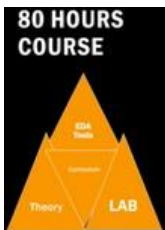
Speakers

Dr. Sameer Shende
Research Professor & Director
University of Oregon.

Dr. Ganesan Narayanasamy
Education and Research Global Leader
IBM.

Dr. Farhang Yazdani
President & Chief Technical Officer
Broadpak Corporation

Dr. Sathyadhyan Chickerur
Professor and Head center for HPC KLE
Technological University, Hubballi.

Dr. Peter Hofstee
Distinguished Research Engineer,
IBM.

Mr. Arjun Nag
Hardware SME,
Tata Consultancy Services

Dr. Abhinandan SP
Assistant Professor, IIT
Ropar.

Dr. Revathi
Professor,
SME in Chip Design.

Many more distinguished academic experts and Industry leaders will speak/present on chip designing using IBM OpenPOWER cores.

Advisory Committee

Advisors

Dr. Sivanantham S
Professor & Dean, SENSE

Dr. Jasmin Pemeena Priyadarisini
Professor & Associate Dean, SENSE

Dr. Jagannadha Naidu K
Assistant Professor & Head,
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