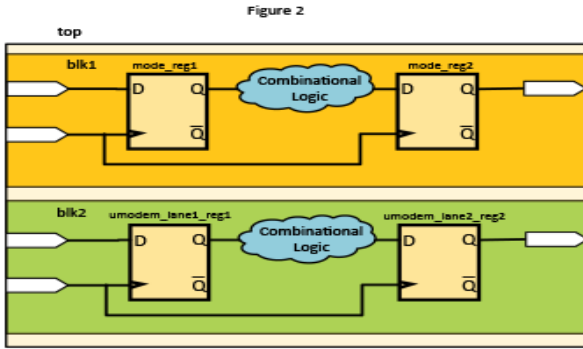
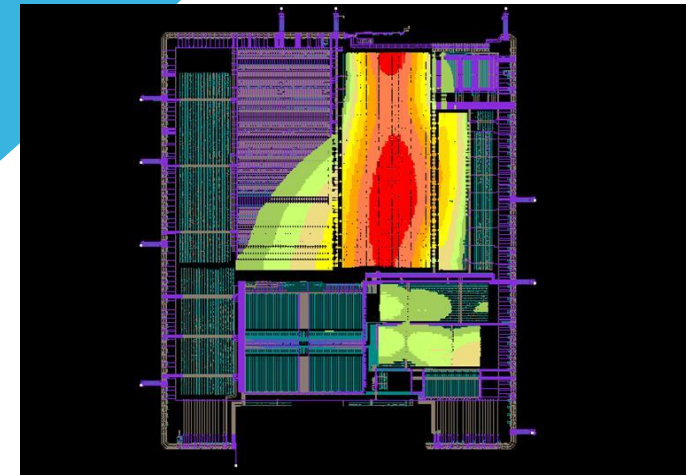


# “VAC - ASIC DESIGN USING CADENCE TOOLS” DEPT.OF MICRO AND NANOELECTRONICS,SENSE



GDSII

DRC / LVS  
Routing



CTS  
Placement

Power Plan  
Floor Plan

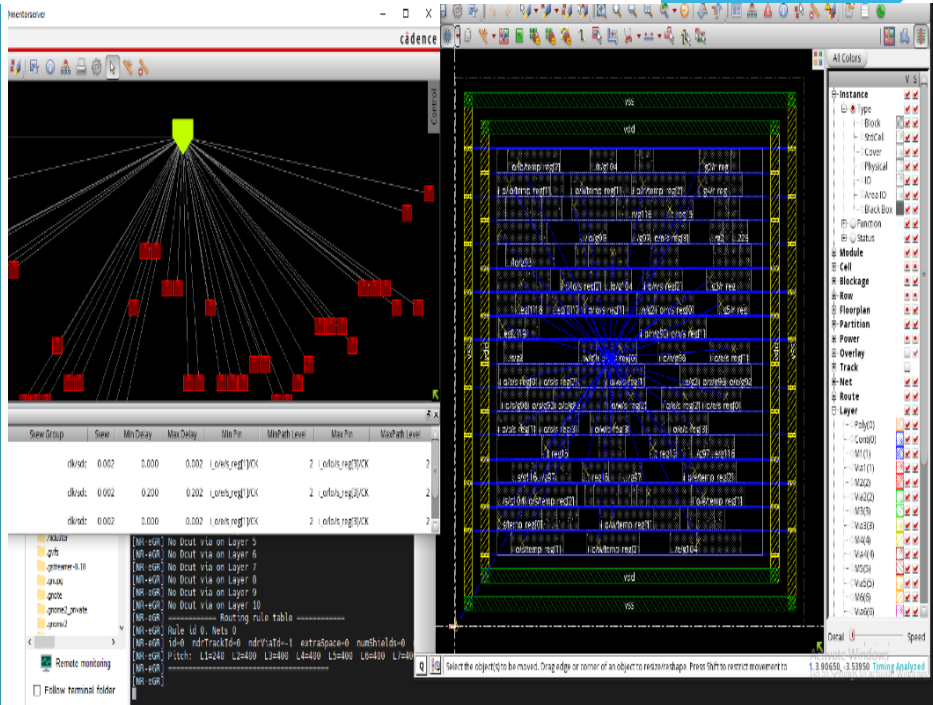
Physical Aware Synthesis  
Synthesis

Simulation  
RTL Design &

Coordinators  
**Dr.Ravi S**  
**Dr.Satheeshkumar**  
**Dr.Rajeev Pankaj**

Registration Link : <https://events.vit.ac.in/>

Specifications





## School of Electronics Engineering

Department of Micro and Nano electronics

### Value Added Course

On

## Hands on ASIC Design using Cadence Tools –VAC - 1555

**About the Course:** The value added course on “**Hands on ASIC Design using Cadence Tools**”, aim to introduce the most demand skills in VLSI. This course deals with the fundamental theory to Practical hand on training in vlsi. This course allows the student to learn from the scratch to write code, design using the CMOS transistors which help them to manage their projects efficiently and make the career as a VLSI design engineer.

### Advisory Committee

Dr. Sivanantham S, Professor & Dean, School of Electronics Engineering

Dr. Noor Mohammed, Professor & HOD  
Department of Communication Engineering, SENSE

Dr. Jagannadha Naidu, HOD,  
Department of Micro and Nano electronics, SENSE

### Faculty Coordinators:

Dr. S Ravi, SENSE  
Email: [msravi@vit.ac.in](mailto:msravi@vit.ac.in)

Dr. Satheeshkumar S , SENSE,

[satheeshkumar.s@vit.ac.in](mailto:satheeshkumar.s@vit.ac.in)

Dr.Rajeev Pankaj Nelapaty,SENSE

[rajeevpankaj@vit.ac.in](mailto:rajeevpankaj@vit.ac.in)

### Highlight of the Course:

- 30 hours Course Duration
- Introduction to Verilog & CMOS
- Practical training: How to write code using Verilog HDL Programming.
- Practical training: How to design Semicustom ASIC Design circuits using Cadence tools.
- Mini Project based on available Lower nm node
- E Certificate  
(Min of 75% attendance & 60% of marks)

### Course Experts:

#### Faculty:

Dr. Harish M Kittur, SENSE.

Dr. Sakthivel R, SENSE

Dr. Ravi S. SENSE

Dr. Satheesh Kumar. SENSE

Dr.Rajeev Pankaj, SENSE

Dr.Jayakrishnan, SENSE

#### Alumni:

Alumni Industry Engineers

**Target Audience:** UG / PG / PhD

**Seats Limited to 60 Participants**

- **Date: 08.7.23(9.00am-7.00pm)**

**09.7.23 (9.00am-7.00pm)**

**15.7.23 (9.00am-7.00pm)**

**Registration Fee:** Rs 1180 (Inclusive of GST) **Registration Link :** <https://events.vit.ac.in/>

### Contct Numbers

9790155650 – Ravi S  
8124424714 –Satheesh  
9043266364 -- Pankaj