VIT
Vellore Institute of Technology

IBM

International Workshop on Chip Design organized by Vellore Institute of Technology, Vellore

June 24th 2024 to July 4th 2024

UNIVERSITY OF **OREGON**

VIT UNIVERSITY

BroadPak
2.5D/3D Technologies

SEMICON DYNAMICS
Semiconductor Ecosystem

OpenPOWER

CDAC
सी डैक

OBJECT AUTOMATION

Why We Are different

Our Eminent speakers

- Dr S D Sudarsan, Executive Director CDAC
- Dr Farhang Yazdani, CTO, Broadpak, USA
- Arjun N, Industry Expert
- Neetha Maria Celin, CDAC India

- Gayathri P, Object Automation
- Ganesan Narayanasamy, OpenPOWER Global Academic and Research Leader
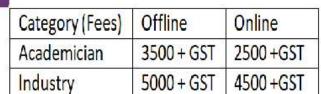- Dr Avesta Sasan, UC Davis
- Mydhily M R, CDAC India

Hybrid hands on sessions & Certification

- Hands on Training on Vega boards, ARIES, FPGA boards.
- interfacing with Various Sensors
- FPGA Programming and Implementation
- Synthesis to GDSII flow using OpenROAD

- EDA Tool (OpenROAD) understanding with LAB Facilities
- Release to Chip Fabrication

Advisors
Dr. Sivanantham S
Professor & Dean, SENSE

Dr. Jasmin Pemeena Priyadarisini
Professor & Associate Dean, SENSE

Faculty Coordinators

1. Dr. Somasundaram D
   Associate Professor
   Mobile: 9791267062
   Email: somasundaram.d@vit.ac.in

For Registration, please visit:
https://events.vit.ac.in

Department of Micro and Nano Electronics

Venue: TT727,
Technology Tower,
VIT, Vellore
Time: 10.00 a.m. – 4.00 p.m.

For more details
please contact,
Mr. Karthikeyan V (T.O) - 9894972399
Department of Micro and Nano Electronics
School of Electronics Engineering
Vellore Institute of Technology, Vellore,
Tamil Nadu, India – 632014.
Last Date to apply : 20.06.2024

- Participants are requested to make their own arrangements for accommodation if possible.
- Certificate will be issued to all the participants.
- based on the prior request, hostel accommodation will be provided with reasonable charges.

Category (Fees)	Offline	Online
Academician	3500 + GST	2500 +GST
Industry	5000 + GST	4500 +GST

SCAN HERE FOR DAY WISE SCHEDULE

SCAN ME