Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING

M. Tech VLSI Design

(M.Tech MVD)

Curriculum

(*2022-2023 admitted students*)

VISION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

Transforming life through excellence in education and research.

MISSION STATEMENT OF VELLORE INSTITUTE OFTECHNOLOGY

World class Education: Excellence in education, grounded in ethics andcritical thinking, for improvement of life.

Cutting edge Research: An innovation ecosystem to extend knowledge andsolve critical problems.

Impactful People: Happy, accountable, caring and effective workforce and students.

Rewarding Co-creations: Active collaboration with national & international industries & universities for productivity and economic development.

Service to Society: Service to the region and world through knowledge and compassion.

VISION STATEMENT OF THE SCHOOL OF ELECTRONICSENGINEERING

To be a leader by imparting in-depth knowledge in Electronics Engineering, nurturing engineers, technologists and researchers of highest competence, who would engage in sustainable development to cater the global needs of industry and society.

MISSION STATEMENT OF THE SCHOOL OF ELECTRONICSENGINEERING

- Create and maintain an environment to excel in teaching, learning and applied research in the fields of electronics, communication engineering and allied disciplines which pioneer for sustainable growth.
- Equip our students with necessary knowledge and skills which enable them to be lifelong learners to solve practical problems and to improve the quality of human life.

M. Tech. VLSI Design

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

1. Graduates will be engineering practitioners and leaders, who would help solve industry's technological problems.

2. Graduates will be engineering professionals, innovators or entrepreneurs engaged in technology development, technology deployment, or engineering system implementation in industry.

3. Graduates will function in their profession with social awareness and responsibility.

4. Graduates will interact with their peers in other disciplines in industry and society and contribute to the economic growth of the country.

5. Graduates will be successful in pursuing higher studies in engineering or management.

6. Graduates will pursue career paths in teaching or research.

M. Tech. VLSI Design

PROGRAMME OUTCOMES (POs)

PO_01: Having an ability to apply mathematics and science in engineering applications.

PO_02: Having an ability to design a component or a product applying all the relevant standards and with realistic constraints, including public health, safety, culture, society and environment

PO_03: Having an ability to design and conduct experiments, as well as to analyse and interpret data, and synthesis of information

PO_04: Having an ability to use techniques, skills, resources and modern engineering and IT tools necessary for engineering practice

PO_05: Having problem solving ability- to assess social issues (societal, health, safety, legal and cultural) and engineering problems

PO_06: Having adaptive thinking and adaptability in relation to environmental context and sustainable development

PO_07: Having a clear understanding of professional and ethical

responsibility

PO_08: Having a good cognitive load management skills related to project management and finance

M. Tech. VLSI Design

PROGRAMME SPECIFIC OUTCOMES (PSOs)

On completion of M. Tech. (VLSI Design) programme,
graduates will be able to

PSO1: Apply advanced concepts in Physics of semiconductor devices to design VLSI Systems.

PSO2: Design ASIC and FPGA based systems using industry standard tools.

PSO3: Solve research gaps and provide solutions to socio-economic, and environmental problems.

Master of Technology in VLSI Design

School of Electronics Engineering

Programme Credit Structure	**Credits**
Discipline Core Courses	24
Skill Enhancement Courses	05
Discipline Elective Courses	12
Open Elective Courses	03
Project/ Internship	26
Total Graded Credit Requirement	70

Discipline Core Courses **24**

		L	**T**	**P**	**C**
MVLD501L	Physics of VLSI Devices	3	0	0	3
MVLD502L	Digital IC Design	3	0	0	3
MVLD503L	Digital Design with FPGA	2	0	0	2
MVLD503P	Digital Design with FPGA Lab	0	0	2	1
MVLD504L	Analog IC Design	3	0	0	3
MVLD504P	Analog IC Design Lab	0	0	2	1
MVLD505L	ASIC Design	3	0	0	3
MVLD505P	ASIC Design Lab	0	0	2	1
MVLD506L	VLSI Testing and Testability	3	0	0	3
MVLD506P	VLSI Testing and Testability Lab	0	0	2	1
MVLD507L	IC Technology	3	0	0	3

Skill Enhancement Courses **05**

MENG501P	Technical Report Writing	0	0	4	2
MSTS501P	Qualitative Skills Practice	0	0	3	1.5
MSTS502P	Quantitative Skills Practice	0	0	3	1.5

Discipline Elective Courses **12**

MVLD601L	Computer Aided Design for VLSI	3	0	0	3
MVLD602L	Low Power IC Design	3	0	0	3
MVLD603L	VLSI Verification Methodologies	3	0	0	3
MVLD604L	Scripting Languages for VLSI Design Automation	3	0	0	3
MVLD605L	Advanced Computer Arithmetic	3	0	0	3
MVLD606L	Mixed Signal IC Design	3	0	0	3
MVLD607L	RFIC Design	3	0	0	3
MVLD608L	VLSI Digital Signal Processing	3	0	0	3
MVLD609L	System-on-Chip Design	3	0	0	3
MVLD610L	Nanoscale Devices and Circuit Design	3	0	0	3
MVLD611L	Advanced Computer Architecture	3	0	0	3
MVLD612L	Micro Sensors and Interface Electronics	3	0	0	3
MVLD613L	System Design with FPGA	3	0	0	3
MVLD614L	DSP Architectures	3	0	0	3
MVLD615L	Memory Design and Testing	3	0	0	3

Open Elective Courses **03**

Engineering Disciplines | Social Sciences

Project and Internship **26**

MVLD696J	Study Oriented Project	02
MVLD697J	Design Project	02
MVLD698J	Internship I/ Dissertation I	10
MVLD699J	Internship II/ Dissertation II	12

Course Code	Course Title	L	T	P	C
MVLD501L	Physics of VLSI Devices	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Expound the fundamentals of intrinsic, extrinsic semiconductors with carrier concentration, Modeling and physics of various carrier current transport mechanisms.
2. Introduce detailed physics and modeling of PN Junction, MOS capacitors, and MOSFETs
3. Review and discuss in detail the short channel effects and the issues of UDSM transistors

Course Outcomes:

At the end of the course the student will be able to

1. Design extrinsic semiconductors with specific carrier concentrations and, understand the band Structure and diagrams of semiconductors.
2. Calculate and model the carrier transport mechanism in semiconductors
3. Design of PN- junctions for given specifications
4. Understand the MOS capacitors
5. Understand the compact models of MOSFETs
6. Design of UDSM transistors to mitigate the short channel effects

Module:1	**Semiconductor Physics**	**5 hours**

Energy bands in solids - Intrinsic and Extrinsic semiconductors - Direct and Indirect bandgap -Density of states - Fermi distribution -Free carrier densities - Boltzmann statistics - Thermal equilibrium.

Module:2	**Carrier Transport in Semiconductors**	**4 hours**

Current flow mechanisms: Drift current, Diffusion current - Mobility of carriers - Current density equations - Continuity equation.

Module:3	**P-N Junctions**	**5 hours**

Thermal equilibrium physics - Energy band diagrams - Space charge layers - Poisson equation - Electric fields and Potentials - p-n junction under applied bias - Static current-voltage characteristics of p-n junctions - Breakdown mechanisms.

Module:4	**MOS Capacitor**	**8 hours**

Accumulation - Depletion - Strong inversion - Threshold voltage - Contact potential - Gate work function - Oxide and Interface charges - Body effect - C-V characteristics of MOS

Module:5	**MOSFETs and Compact Models**	**8 hours**

Drain current - Saturation voltage - Sub-threshold conduction - Effect of gate and drain voltage on carrier mobility - Compact models for MOSFET and their implementation in SPICE: Level 1, 2 and 3 - MOS model parameters in SPICE.

Module:6	**Scaling and Short Channel Effects**	**6 hours**

Effect of scaling - Channel length modulation - Punch-through - Hot carrier degradation - MOSFET breakdown - Drain-induced barrier lowering.

Module:7	**UDSM Transistor Design Issues**	**7 hours**

Effect of tox - Effect of high-k and low-k dielectrics on the gate leakage and Source and drain leakage - tunneling effects - Different gate structures in UDSM - Impact and reliability challenges in UDSM.

Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	Ben G. Streetman and S. Banerjee, Solid State Electronic Devices, 2015, Seventh Edition, Pearson Education, U.S.		
2	J.P. Colinge and C. A. Colinge, Physics of Semiconductor Devices, 2017, Kluwer Academic Publishers, U.S.		
Reference Books			
1.	Y.P. Tsividis and Colin McAndrew, Operation and Modelling of the MOS Transistor, 2011, Third Edition, Oxford University Press, U.S.		
2	M K Achutan and K N Bhatt, Fundamental of Semiconductor Devices, 2017, McGraw Hill Education, U.S.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD502L	Digital IC Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Apply the models for state-of-the-art VLSI components, fabrication steps, and hierarchical design flow and semiconductor business economics to judge the manufacturability of a design and assess its manufacturing costs.
2. Focus on the systematic analysis and design of basic digital integrated circuits in CMOS technology.
3. Enhance problem solving and creative circuit design techniques.
4. Emphasize on the layout design of various digital integrated circuits.
5. Focus on the methodologies and design techniques related to digital integrated circuits.

Course Outcome

At the end of the course the student will be able to

1. Understand design metric and MOS physics
2. Design layout for various digital integrated circuits.
3. Design the CMOS inverter with optimized power, area and timing.
4. Design static and dynamic digital CMOS circuits.
5. Understand the timing concepts in latch and flip-flops.
6. Design CMOS memory arrays, understand interconnect and clocking issues.

Module:1	Introduction	3 hours

Issues in Digital IC Design- Quality Metrics of a Digital Design - MOS Transistor Theory.

Module:2	CMOS Fabrication and Layout	7 hours

CMOS Process Technology N-well, P-well process, Stick diagram for Boolean functions, Optimization using Euler Theorem, Layout Design Rules

Module:3	The CMOS Inverter	5 hours

Static CMOS Inverter- Static and Dynamic Behavioural Practices of CMOS Inverter – Noise Margin. Components of Energy and Power – Switching -Short-Circuit and Leakage Components. Technology scaling and its impact on the inverter metrics - Passive and Active Devices.

Module:4	Static & Dynamic CMOS Design	8 hours

Delay Calculation using Logical Effort, Complementary CMOS -Ratioed Logic (Pseudo NMOS, DCVSL) - Pass Transistor Logic - Transmission gate logic - Dynamic Logic Design Considerations - Speed and Power Dissipation of Dynamic logic -Signal integrity issues - Domino Logic.

Module:5	CMOS Sequential Logic Circuit Design	5 hours

Introduction - Static Latches and Registers - Dynamic Latches and Registers - Pulse Based Registers - Sense Amplifier based registers -Latch vs. Register based pipeline structures.

Module:6	Designing Memory & Array structures	7 hours

SRAM and DRAM Memory Core - memory peripheral circuitry - Memory reliability and yield - Power dissipation in memories.

Module:7	Interconnects and Timing Issues	8 hours

Resistive, Capacitive and Inductive Parasitics - Computation of R, L and C for given interconnects - Buffer Chains - Timing classification of digital systems - Synchronous Design - Origins of Clock Skew/Jitter and impact on Performance - Clock Distribution Techniques - Latch based clocking - Synchronizers and Arbiters -Clock Synthesis and Synchronization using a Phase Locked Loop.

Module:8	Contemporary Issues	2 hours

	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Jan M. Rabaey, AnanthaChadrakasan and BorivojeNikolic, Digital Integrated Circuits: A Design Perspective, 2016, Second Edition, PHI.
2.	Neil.H, E.Weste, David Harris and Ayan Banerjee, CMOS VLSI Design: A Circuit and Systems Perspective, 2011, Fourth Edition, Pearson Education.
Reference Books	
1.	Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis and Design, 2014, Fourth Edition, McGraw-Hill.
2.	Sorab K Gandhi, VLSI Fabrication Principles: Si and GaAs, 2010, Second Edition, John Wiley and Sons.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD503L	Digital Design with FPGA	2	0	0	2
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

This course is aimed to

1. Understand the various abstraction level in Verilog HDL.
2. Model the complex combinational and sequential circuits with Verilog HDL
3. Provide in depth understanding of state machine design and modeling using Verilog HDL.
4. Understand about different FPGA Architecture like Xilinx and ALTERA and RAM and controller design.

Course Outcome

After completion of the course the student will be able to:

1. Design and implement digital circuits using Data Flow & Structural Modeling.
2. Design and develop combinational circuits using data flow approach
3. Design and implement sequential digital circuits using Behavioral Modeling.
4. Understand and develop data-path and controller design
5. Develop and test memory sub-system.
6. Build digital designs using FPGA.

Module:1	**Verilog HDL – Data Flow & Structural Modeling**	**6 hours**

Lexical Conventions - Ports and Modules – Data Types - Operators - Gate Level Modeling - Data Flow Modeling - - Test Bench.

Module:2	**Design and Modeling of data path logic**	**4 hours**

Ripple carry Adders – Carry look ahead adder – Unsigned binary Multipliers

Module:3	**Verilog HDL – Behavioral Modeling**	**4 hours**

Behavioral level Modeling- Procedural Assignment Statements- Blocking and Non-Blocking Assignments -Tasks & Functions - System Tasks & Compiler Directives

Module:4	**Design and Modeling of Sequential Circuits**	**4 hours**

FSM modeling of Sequence detector - Serial adder - Vending machine

Module:5	**Design and Modeling of Datapath and Controller logic**	**3 hours**

Case Study: Binary Counter - Bus Protocol

Module:6	**Modeling of FIFO and Memory**	**3 hours**

Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM

Module:7	**FPGA Architecture**	**4 hours**

Types of Programmable Logic Devices: PLA, PAL, CPLD - FPGA Architecture - Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA - Xilinx / Intel / Actel FPGA Architecture – Case Study

Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**30 hours**

Text Book(s)

1. Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, 2015, Second Edition, Create Space Independent Publishing Platform.

2.	Michael D Ciletti, Advanced Digital Design with the Verilog HDL, 2011, Second Edition, Prentice-Hall.		
Reference Books			
1.	Wayne Wolf, FPGA Based System Design, 2011, Prentices Hall Modern Semiconductor Design Series.		
2.	Charles H Roth Jr, Lizy Kurian John and Byeong Kil Lee, Digital Systems Design using Verilog, 2016, First Edition, Cengage Learning.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD503P	Digital Design with FPGA Lab	0	0	2	1
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

This course is aimed to

1. Model the complex combinational and sequential circuits using Verilog HDL

Course Outcome

After completion of the course the student will be able to:

1. Design and optimize complex combinational and sequential digital circuits using Verilog.
2. Implement the designed digital design using FPGA.

	Indicative Experiments	
1.	Many ink-jet printers have six cartridges for different colored ink: black, cyan, magenta, yellow, light cyan and light magenta. A multibit signal in such a printer indicates selection of one of the colors. Write a data flow Verilog model for a decoder for use in the inkjet printer described above. The decoder has three input bits representing the choice of color cartridge and six output bits, one to select each cartridge. Verify the output of the design using test bench by simulating in Modelsim Simulator. Implement the design in ALTERA DE2-115 Board and verify it's functionality.	4 hours
2.	Write a behavioral Verilog code to divide the ALTERA DE2-115 Board clock frequency 50MHz by 40MHZ, 30MHz, 20 MHz, 10MHz. Display each of the output using LEDs available in the board.	4 hours
3.	Design and implement a circuit on the DE2-115 board that acts as a time-of-day clock. It should display the hour (from 0 to 23) on the 7-segment displays HEX7−6, the minute (from 0 to 60) on HEX5−4 and the second (from 0 to 60) on HEX3−2. Use the switches SW15−0 to preset the hour and minute parts of the time displayed by the clock.	4 hours
4.	We wish to implement a finite state machine (FSM) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s or four consecutive 0s. There is an input w and an output z. Whenever w = 1 or w = 0 for four consecutive clock pulses the value of z has to be 1; otherwise, z = 0. Overlapping sequences are allowed, so that if w = 1 for five consecutive clock pulses the output z will be equal to 1 after the fourth and fifth pulses. Design and Implement the design using DE2-115 Board.	8 hours
5.	Write a behavioral Verilog code to design FIFO with the following specification d_in: input data; 8 bit width is considered d_out: output data; 8 bit width is considered · w_en: write enable signal r_en: read enable signal r_next_en: read next enable w_next_en: write next enable w_clk: write clock; 10 MHz for this design r_clk: read clock; 50 MHz for this design w_ptr: write address pointer; 4 bit to address depth of 16 · r_ptr: read address pointer; 4 bit to address depth of 16 · ptr_diff: address pointer difference; 4 bit width f_full_flag: FIFO full flag; asserted when FIFO is full · f_empty_flag: FIFO empty flag; asserted when FIFO is empty Use Dual Port RAM available in ALTERA IP library to realize the FIFO. Implement the design using ALTERA DE2-115 board.	10 hours

		Total Laboratory Hours	**30 hours**
Mode of Assessment: Continuous Assessment and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD504L	Analog IC Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Analyze and design single-ended and differential IC amplifiers.
2. Understand the relationships between devices, circuits and systems.
3. Emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.

Course Outcome

At the end of the course the student will be able to

1. Analyze low-frequency characteristics of single-stage amplifiers and differential amplifiers
2. Analyze high-frequency response and noise of amplifiers.
3. Understand the feedback concepts.
4. Analyze and Design of High Gain Amplifiers.
5. Understand stability analysis and frequency compensation techniques of amplifiers.
6. Understand the basic concepts, non-idealities and applications of PLLs.

Module:1	**Current source and Amplifier design:**	**8 hours**

MOS Device models, MOS Current Sources and Sinks, Current Mirror: Basic Current Mirrors, Cascode current Mirrors. Bandgap references. Single stage Amplifies: Basic concepts, Common Source stage, Common Gate stage, Cascode stage. Differential stage: Single ended and Differential operation. Basic Differential Pair.

Module:2	**Frequency response and Noise analysis of Amplifiers:**	**8 hours**

Miller effect, Frequency response of Common Source stage, Common Gate stage, Cascode stage and Differential pair. Noise in Amplifiers: Common Source stage, Common Gate stage, Cascode stage, Differential pair. Noise Bandwidth.

Module:3	**Feedback Amplifiers:**	**7 hours**

Ideal feedback equation, Gain sensitivity, Effect of Negative Feedback on Distortion, Types of Feedback Amplifiers. Feedback configurations: voltage-voltage, current-voltage, current-current, voltage-current feedback. Practical configurations and Effect of loading.

Module:4	**Operational Amplifier**	**8 hours**

Common mode Feedback circuits, Op Amp CMRR requirements, Need for Single and Multistage amplifiers, Effect of loading in Differential stage. Performance Analysis: DC gain, Frequency response, Noise, Mismatch, Slew rate of cascode and two stage Op Amps, Fully Differential Op Amps, Common-Mode feedback loop stability.

Module:5	**Stability analysis**	**4 hours**

Basic Concepts, Instability and the Nyquist Criterion, Stability Study for a Frequency-Selective Feedback Network, Effect of Pole Locations on Stability

Module:6	**Frequency compensation**	**4 hours**

Frequency Compensation: Concepts and Techniques for Frequency Compensation – Dominant pole, Miller Compensation, Compensation of Miller RHP Zero, Nested Miller, Compensation of two stage OP Amps.

Module:7	**Phase Locked Loops**	**4 hours**

Problem of Lock acquisition, Phase Detector, Basic PLL and its dynamics, Charge-pump PLL, Non-ideal effects in PLL: PFD/CL non idealities, Jitter, Delay Locked Loop, Applications.

Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)			
1.	Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2017, Second Edition, McGraw-Hill.		
2.	David Johns and Ken Martin, Analog Integrated Circuit Design, 2012, Second Edition, John Wiley & Sons, Inc.		
Reference Books			
1.	Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2010, Second Edition, Oxford University Press, UK.		
2.	R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, 2010, Third Edition, IEEE Press Series on Microelectronic Systems, Wiley Publications.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD504P	Analog IC Design Lab	0	0	2	1
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Analyze and design single-ended and differential IC amplifiers.
2. Understand the relationships between devices, circuits and systems.
3. Emphasize the design of practical amplifiers, small systems and their design parameter trade-offs.

Course Outcome

At the end of the course students will be able to

1. Design and characterize amplifiers according to design specifications in industry standard EDA tool.

Indicative Experiments

1.	Simulation of MOSFET IV Characteristics, Second order parameters	2 hours
2.	CMOS Inverter - DC, AC, Transient Analysis	2 hours
3.	Analysis and Design of Common Source Amplifier with Diode Connected Load and Suggest a Circuit to achieve higher gain.	4 hours
4.	Analysis and Design of Common Gate Amplifier with Resistive load and Current Source load. Justify the results in terms of input impedance of the circuit.	4 hours
5.	Analysis and Design of Simple Current Mirror and Suggest a circuit to minimize the error in the output current.	4 hours
6.	Analysis and Design of Differential Amplifier with Active load and Current Source Load.	4 hours
7.	Analysis and Design of Cascode Amplifier and Suggest a Circuit to overcome Voltage Headroom Limitation.	4 hours
8.	Analysis and Design of Two-Stage Opamp with Frequency Compensation.	6 hours
	Total Laboratory Hours	**30 hours**

Mode of Evaluation: Mode of Assessment: Continuous Assessment and Final Assessment Test

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD505L	ASIC Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course aimed to

1. Understanding of HDL coding guidelines and synthesizable HDL constructs.
2. Understand the RTL synthesis Flow with respect to different cost functions.
3. Analyse Static Timing requirements for ASIC design.
4. Discuss the guidelines at each abstraction level in physical design
5. Understand the importance of physical design verification

Course Outcome

At the end of the course the student will be able to

1. Design digital systems by adhering to synthesizable HDL constructs.
2. Synthesize the given design by considering various constraints and to optimize the same.
3. Understand various timing parameters and perform Static Timing Analysis for ASIC design
4. Compare OCV modelling techniques.
5. Perform physical design by adhering to guidelines.
6. Understand the importance of physical design verification.

Module:1	**ASIC Design Methodology & Design Flow**	**4 hours**
Implementation Strategies for Digital ICs: Custom IC Design- Cell-based Design Methodology - Array based implementation approaches - Traditional and Physical Compiler based ASIC Flow.		
Module:2	**Verilog HDL Coding Style for Synthesis**	**8 hours**
HDL Coding style – Guidelines and Recommendation - FSM Coding Guideline and Coding Style for Synthesis. HDL Coding style for Datapath and Control Logic Design.		
Module:3	**RTL Synthesis**	**6 hours**
RTL synthesis Flow – Synthesis Design Environment & Constraints – Architecture of Logic Synthesizer - Technology Library Basics– Components of Technology Library –Synthesis Optimization- Technology independent and Technology dependent synthesis- Data path Synthesis – Low Power Synthesis - Formal Verification.		
Module:4	**Basic Timing Analysis**	**7 hours**
Timing Parameter Definition – Setup Timing Check- Hold Timing Check- Multicycle Paths- Half-Cycle Paths- False Paths		
Module:5	**Advanced Timing Analysis**	**5 hours**
Clock skew optimization – On-Chip Variations- AOCV-POCV-Time Borrowing- Setup and Hold Violation Fixing.		
Module:6	**Physical Design**	**8 hours**
Detailed steps in Physical Design Flow- Guidelines for Floor plan, Placement, CTS and routing– ECO flow – Signal Integrity Issues.		
Module:7	**Physical Design Verification**	**5 hours**
Timing Sign-off, Physical Verification – Signoff DRC and LVS, ERC, IR Drop Analysis, Electro-Migration Analysis and ESD Analysis.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1. Vaibbhav Taraate, ASIC Design and Synthesis RTL Design Using Verilog, 2021, First Edition, Springer, Singapore.
2. J. Bhasker and Rakesh Chadha, Static Timing Analysis for Nanometer Designs,

	2010, First Edition, Springer, USA.		
Reference Books			
1.	Khosrow Golshan, PHYSICAL DESIGN ESSENTIALS An ASIC Design Implementation Perspective, 2010, First Edition, Springer.		
2.	Michael John Sebastian Smith, Application-Specific Integrated Circuits, 2002, First Edition, Addison Wesley.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD505P	ASIC Design Lab	0	0	2	1
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. To apply theoretical knowledge gained in the ASIC Design course and get hands-on experience of the topics.

Course Outcome

At the end of the course the student will be able to

1. Design, simulate and synthesize complex digital system
2. Analyse and fix the timing violations
3. Design ASIC based digital systems using industry standard EDA tools.

Indicative Experiments		
1.	Design of Digital Architecture for given specification	6 hours
2.	Logical Synthesis of Digital Architecture	6 hours
3.	Netlist Optimization, GLS and Formal Verification	6 hours
4.	Physical Synthesis of Digital Architecture	6 hours
5.	Physical Verification of Digital Architecture	6 hours
	Total Laboratory Hours	**30 hours**

Mode of Assessment: Continuous Assessment and Final Assessment Test

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD506L	VLSI Testing and Testability	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives :

The course is intended to

1. Introduce the concept of modeling and simulation of logic and memory testing.
2. Familiarize different design for testability techniques for improving the yield of IC design.

Course Outcomes :

After completion of the course students will be able to

1. Understand the Fault Models and generate test patterns for digital circuits.
2. Apply DFT techniques viz. scan based testing, BIST and boundary scan for improving testability
3. Use of test vector compression and test response compaction techniques to reduce test time and memory storage
4. Test, diagnose and repair memory faults in SoC

Module:1	VLSI Testing and Fault Modelling	6 hours

Importance of Testing - Testing during the VLSI Lifecycle - Challenges in the VLSI Testing: Test Generation - Fault Models – Levels of Abstraction in VLSI Testing - Historical Review of VLSI Test Technology - Fault Equivalence - Fault Dominance - Fault Collapsing - Check point Theorem.

Module:2	Fault Simulation and Test Generation	5 hours

Fault Simulation: Serial, Parallel, Deductive, Concurrent, Fault sampling - Combinational Test Generations -ATPG for Combinational Circuits - D-Algorithm – Classification of faults.

Module:3	Design for Testability	7 hours

Testability Analysis: SCOAP measures for Combinational Circuits - Design for Testability Basics - Ad Hoc Approach - Structured Approach - Scan Cell Designs - Scan Architectures - Scan Design Rules - Scan Design Flow – Special Purpose Scan Designs

Module:4	Logic Built-in Self-Test	7 hours

BIST Design Rules - Test Pattern Generation: Exhaustive Testing, Pseudo-Random Testing, Pseudo-Exhaustive Testing, Delay Fault Testing - Output Response Analysis - Logic BIST Architectures

Module:5	Test Compression and Boundary scan	6 hours

Test Stimulus Compression Techniques: Linear-Decompression-Based Schemes – Broadcast based compression schemes. Test Response Compaction - Digital Boundary Scan (IEEE Std. 1149.1): Test Architecture and Operations - On-Chip Test Support with Boundary Scan - Board and System-Level Boundary-Scan Control Architectures – IJTAG architectures.

Module:6	Memory Testing and Built-In Self-Test	6 hours

RAM Functional Fault Models and Test Algorithms - RAM Fault Simulation and Test Algorithm Generation - Memory Built-In Self-Test

Module:7	Memory Diagnosis and Built-In Self-Repair	6 hours

BIST with Diagnostic Support - RAM Defect Diagnosis and Failure Analysis - Built-In Self-Repair

Module:8	Contemporary Issues	2 hours

	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, VLSI Test Principles and Architectures, 2013, The Morgan Kaufmann.
2.	M. Bushnell, Vishwani Agrawal - Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, 2006, Springer.
Reference Books	
1.	Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "System-on-chip Test Architectures: Nanometer Design for Testability", 2008, Morgan Kaufmann Publishers.
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test	

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD506P	VLSI Testing and Testability Lab	0	0	2	1
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is intended to

1. Introduce the concept of modeling and simulation of logic and memory testing
2. Familiarize different design for testability techniques for improving the yield of IC design using industry standard EDA tools

Course Outcomes:

After completion of the course the student will be able to:

1. Generate test patterns and perform fault simulation for digital logic and memory circuits.
2. Apply DFT techniques viz. scan based testing, BIST and boundary scan for improving testability using EDA tools.

Indicative Experiments		
1.	Fault Simulation and Test generation for combination circuits	4 hours
2.	Clock and reset rule check at RTL	4 hours
3.	Scan Chain Insertion, DRC and ATPG	2 hours
4.	At-Speed Patterns and On-Chip Clock Controllers (LoS and LoC)	4 hours
5.	Advanced fault modeling	2 hours
6.	SDF annotated simulation	4 hours
7.	Boundary scan test	4 hours
8.	Testing of memories (BIST insertion, validation and BIST repair)	6 hours
	Total Laboratory Hours	**30 hours**

Mode of Assessment: Continuous Assessment and Final Assessment Test

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD507L	IC Technology	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course intended to

1. Introduce the process involved in semiconductor manufacturing, lithography and fabrication.
2. Model the oxidation growth rate & to understand oxidation process and the process of diffusion and to expound the Ion Implantation process.
3. Explain the thin film deposition process and review the difference between MOS and Bipolar Process Integration.

Course Outcome

At the end of the course the student will be able to

1. Understand the process involved in semiconductor manufacturing, lithography and fabrication.
2. Understand the various lithography techniques used for pattern transfer.
3. Apply models for understanding the oxidation growth.
4. Understand the diffusion mechanism in semiconductors.
5. Understand the process involved in thin film deposition.
6. Analyse the difference between MOS and Biploar Process

Module:1	**Crystal Growth**	**5 hours**

Introduction to Semiconductor Manufacturing and fabrication, Clean Room types and Standards, Physics of the Crystal growth, wafer fabrication and basic properties of silicon wafers.

Module:2	**Lithography**	**7 hours**

The Photolithographic Process, Photomask Fabrication, Comparison between positive and negative photoresists, Exposure Systems, Characteristics of Exposure Systems, E-beam Lithography, X- ray lithography

Module:3	**Thermal Oxidation of Silicon**	**6 hours**

The Oxidation Process, Modeling Oxidation, Masking Properties of Silicon Dioxide, Technology of Oxidation, Si-SiO_2 Interface

Module:4	**Diffusion and Ion Implantation**	**7 hours**

The Diffusion Process, Mathematical Model for Diffusion, Constant-, The Diffusion Coefficient, Successive Diffusions, Diffusion Systems, Implantation Technology, Mathematical Model for Ion Implantation, Selective Implantation, Channeling, Lattice Damage and Annealing, Shallow Implantations.

Module:5	**Thin film deposition, contacts, packaging and yield**	**7 hours**

Chemical Vapor Deposition, Physical Vapor Deposition, Epitaxy, Metal Interconnections and Contact Technology, Silicides and Multilayer-Contact Technology, Copper Interconnects and Damascene Processes, Wafer Thinning and Die Separation, Die Attachment, Wire Bonding, Packages, Yield

Module:6	**MOS Process Integration**	**5 hours**

Basic MOS Device Considerations, MOS Transistor Layout and Design Rules, Complementary MOS (CMOS) Technology

Module:7	**Bipolar Process Integration**	**6 hours**

Isolation Techniques in BJT fabrication, Advanced Bipolar Structures, Other Bipolar Isolation Techniques. Deep Submicron Processes, Low-Voltage/Low-Power CMOS/BiCMOS Processes. Future Trends and Directions of CMOS/BiCMOS Processes

Module:8	**Contemporary Issues**	**2 hours**

	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	S.M. Sze, VLSI technology, 2017, Second Edition, Tata McGraw-Hill.
2.	R.C. Jaeger, Introduction to microelectronic fabrication, 2013, Second Edition, Prentice Hall.
Reference Books	
1.	S.A. Campbell, The science and engineering of microelectronics fabrication, 2012, Second Edition, Oxford University Press, UK.
2.	Simon M. Sze, Gary S. May, Fundamentals of Semiconductor Fabrication, 2011,Wiley.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD601L	Computer Aided Design for VLSI	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Acquire the fundamentals of graphs, the relevance and, their applications to VLSI design automation.
2. Introduce the students with relevant examples the estimation of computational complexity and the general classes of computational problems.
3. Explain With relevant examples and algorithms demonstrate partitioning, floor planning, area routing, clock routing and pin assignment of physical design flow

Course Outcome

At the end of the course students will be able to

1. Develop the graphs for the given problems;
2. Determine and analyse the computational complexity of physical design algorithms;
3. Create the partition for a given design.
4. Develop and change the floorplans in an abstract manner and use computer algorithms to make large and optimized floorplans
5. Create optimized placements on the silicon chip and perform complex routing using algorithms and computer codes.
6. Design clock trees to distribute the clock signals on the chip while satisfying various constraints like clock skew and wire length.

Module:1	**Introduction to graph theory**	**5 hours**
Y Chart- Physical design top down flow- Review of graph theory: complete graph, connected graph, sub graph, isomorphism, bi partite graph tree.		
Module:2	**Computational complexity of algorithms**	**4 hours**
Big-O notation- Class P- class NP -NP-hard- NP-complete.		
Module:3	**Partitioning**	**6 hours**
Problem formulation- Group Migration Algorithm: Kernighan-Lin Simulated annealing based Partitioning.		
Module:4	**Floor planning**	**6 hours**
Stock Meyer algorithm- Wong-Liu algorithm (Normalized polish expression)- Integer Linear Programming (ILP) based floor planning.		
Module:5	**Pin Assignment and Placement**	**7 hours**
Pin Assignment: Concentric circle mapping, Topological pin assignment- Power and ground routing. Placement: Wire length estimation models for placement - Quadratic placement- Sequence pair technique.		
Module:6	**Routing**	**8 hours**
Routing: Grid routing- Maze routing- Line Probe algorithms, Weighted Steiner tree approach. Global routing: Rectilinear routing(spanning tree, steiner tree)-Dijkstra's algorithm-routing by ILP Detailed routing: Problem formulation- Two layer channel routing : Left Edge algorithm, Dogleg router- Net Merge channel router - Three-layer channel routing - HVH, VHV router- Introduction to switch box routing.		
Module:7	**Clocking Tree Topologies**	**7 hours**
Clocking tree topologies: H-tree, Xtree- Method of Means and Medians (MMM)- recursive geometric matching- Elmore delay model to calculate skew- Buffer insertion in clock trees- Exact Zero skew clock routing algorithm. Clock mesh topologies: uniform and non-uniform mesh.		
Module:8	**Contemporary Issues**	**2 hours**

	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Andrew B. Kahng, Jens Lienig, Igor L. Markov, JinHu,VLSI Physical Design: From Graph Partitioning to Timing Closure, 2011, Springer.
2.	Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, 2011, Springer, India.
Reference Books	
1.	Ganesh M.Magar, Swati R.Maurya Rajesh K.Maurya, Graph Theory & Applications, 2016, Technical Publications.
2.	Brian Christian and Tom Griffiths, Algorithms to Live By: The Computer Science of Human Decisions, 2017, William Collins.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD602L	Low Power IC Design	3	0	0	3
Pre-requisite	MVLD502L	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. To understand the concept of VLSI circuit with low power consumption
2. To design various circuits for optimum power consumption.
3. To provide a broad insight into the methods used to confront the low power issue from lower level (circuit level) to higher levels (system level) of abstraction.
4. To develop a system with multiple supply and threshold voltages applicable for low power DSP applications

Expected Course Outcomes:

At the end of the course the student will be able to:

1. Analyse the need for low power VLSI circuits
2. Estimate the power consumed in the circuits
3. Improve the power at algorithmic and architectural level.
4. Improve the power at RTL level
5. Apply circuit techniques to optimize the power consumption.
6. Analyse and explore the usage of sleep transistors, IP design for low power and inspect non CMOS devices for low power

Module:1	Introduction to Low Power Design Methods	4 hours

Motivation- Context and Objectives-Sources of Power dissipation in Ultra Deep Submicron CMOS Circuits – Static, Dynamic and Short circuit components Effects of scaling on power consumption- Low power design flow- Normalized Figure of Merit – PDP& EDP- Overview of power optimization at various levels.

Module:2	Power Estimation	6 hours

Theoretical background – Calculation of Steady state probability, Transition probability, Conditional probability, Transition probability of correlated inputs, Transition density; Estimation of Switching activity, Estimation of glitching power.

Module:3	Algorithmic and Architecture Level Optimization	7 hours

Computer arithmetic techniques for low power. Software level power optimization. Pipelining, Parallel Processing and retiming approaches for power minimization, Multiple supply voltage for low power ---MVS,DVS.AVS, DFVS, Optimal drivers of high speed low power ICs,

Module:4	Register Transfer Level Optimization	7 hours

Low power clock-Interconnect and layout designs- Low power memory design and low power SRAM architectures- Clock gating, Data gating Bus Encoding techniques, Deglitching for low power.

Module:5	Logic Level and Circuit Level Optimization	6 hours

Transistor variable re-ordering for power reduction, pre-computation, Low power library cell design (GDI). Circuit techniques for reducing power consumption in Adders, Multipliers. Synthesis of FSM for low power.

Module:6	Leakage Power Reduction	8 hours

Leakage power reduction techniques-stacking techniques, sleepy keeper technique, super cut off CMOS, VTCMOS, MTCMOS,DTCMOS- energy constrained and delay constrained. Sleep Transistor Design- switch efficiency, area efficiency, IR drop, normal Vs reverse body bias. Inrush current and current latency. Power gating –course grain and fine grain. Isolation, retention, power down and wake up methods.

Module:7	IP Design for low power	5 hours

Architecture and partitioning, power controller design for the USB OTG- Issues in designing portable power controllers- clocks and resets- Packaging IP for reuse with power intent.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**
Text Book(s)		
1.	Kaushik Roy, Sharat Prasad, Low Power CMOS VLSI circuit design, 2010, Second Edition, John Wiley and Sons Inc.	
2.	Ajit Pal , Low Power VLSI circuits and Systems, 2014, First Edition, Springer, India,	
Reference Books		
1.	Gary K.Yeap, Practical Low Power Digital VLSI Design, 2010, First Edition, Springer, US.	
2.	Jan M.Rabaey, Massoud Pedram, Low power Design methodologies, 2014, First Edition, Springer, US.	
3.	Soudris, Dimitrios, Christrian Pignet, Goutis, Costas, Designing CMOS circuits for low power, 2011, First Edition, Springer, US.	
4.	Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, Kaijian Shi, Low power methodology manual: for system-on-chip design, 2007, Springer Science & Business Media.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.		
Recommended by Board of Studies	28-07-2022	
Approved by Academic Council	No. 67	Date 08-08-2022

Course Code	Course Title	L	T	P	C
MVLD603L	VLSI Verification Methodologies	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. To introduce various verification techniques.
2. To write Testbench using System Verilog.
3. To develop UVM test bench environment

Course Outcome

At the end of the course students will be able to

1. Demonstrate the VLSI verification techniques.
2. Define classes and create objects.
3. Develop design using system verilog
4. Create Verification environment using System Verilog
5. Perceive the UVM Verification environment.
6. Create reusable verification environment using UVM.

Module:1	**Verification Techniques**	**6 hours**
Introduction to Verification - Testing Vs Verification - Verification Technologies - Functional Verification- Code coverage – Functional coverage. Testbench – Linear Testbench - Linear Random Testbench - Self-checking Testbench – Regression - RTL Formal Verification.		
Module:2	**Basic OOP**	**5 hours**
OOP Terminology, Creating Object, object deallocation, copying objects, static variables, Global variables, Inheritance, Polymorphism		
Module:3	**System Verilog – Data Types & Procedural statements**	**7 hours**
Introduction to System Verilog – Literal values-data Types – Arrays – Array methods – Creating new types with typedef – user defined structures – Enumerated types – attributes - operators – expressions - Procedural statements and control flow - Processes in System Verilog – Task and functions – Routine arguments – Returning from a routine		
Module:4	**Connecting Testbench and Design**	**6 hours**
Program, Interface, Stimulus timing, Module interactions, Connecting together, Development of self-checking test environment – Generator, Transactor, Driver, Monitor, Checker, Scoreboard		
Module:5	**Randomization, Assertion and Coverage**	**7 hours**
Randomization in system Verilog, Constraints, Functional coverage, cross coverage, cover groups, Assertions.		
Module:6	**Universal Verification Methodology**	**6 hours**
Introduction to UVM - Verification components - Transaction level modeling		
Module:7	**UVM – Verification Environments**	**6 hours**
Developing reusable verification components - Using Verification components – Developing reusable verification environment – Register classes.		
Module:8	**Contemporary issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	Vanessa R. Copper, “Getting started with UVM: A Beginner’s Guide”, 2013, First Edition, Verilab Publishing.
2.	Christian B Spear, “System Verilog for Verification: A guide to learning the Testbench language features”, 2012, Third Edition, Springer publications.

Reference Books

1.	Janick Bergeron, “Writing Testbenches using System Verilog” 2006, Synopsys Inc., Springer Publications.

3.	Ray Salmei, “The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology” 2013, First Edition, Boston Light Press.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD604L	Scripting Languages for VLSI Design Automation	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. To write scripts in the LINUX environment.
2. To study the principles of Scripting Languages like Perl, TCL and Python.
3. To write the scripts for automation using the languages like Perl, TCL and Python.

Course Outcomes:

At the end of the course the student will be able to

1. Explain and apply commands in LINUX environment.
2. Develop and execute the Perl scripts.
3. Analyze and Handle files, directories and manage processes using Perl scripts.
4. Use TCL scripts for automation.
5. Build TCL scripts to Handle files, directories and manage process.
6. Develop Python scripts to interpret files and directories.

Module:1	**LINUX Basics**	**5 hours**
Introduction to Linux, File System of Linux, General usage of Linux Kernel and Basic Commands, Linux users and group, Permissions for file, directory and users, Searching a file and directory, zipping and unzipping concepts.		
Module:2	**PERL Basics**	**7 hours**
History and Concepts of PERL - Scalar Data - Arrays and List Data - Control structures – Hashes - Basics I/O - Regular Expressions – Functions - Miscellaneous control structures - Formats.		
Module:3	**Advanced Topics in PERL**	**6 hours**
Directory access - File and Directory manipulation - Process Management - Packages and Modules.		
Module:4	**TCL Basics**	**7 hours**
An Overview of TCL and Tk -Tcl Language syntax – Variables – Expressions – Lists - Control flow – procedures - Errors and exceptions - String manipulations.		
Module:5	**Advanced Topics in TCL**	**6 hours**
Accessing files- Processes. Applications - Controlling Tools - Basics of Tk.		
Module:6	**Python Basics**	**6 hours**
Introduction to Python – Using Python interpreter – Brief tour on standard library - Control flow Tools – Data structures – Regular Expressions.		
Module:7	**Advanced Topics in Python**	**6 hours**
Input and Output – Errors and Exceptions – Classes – Modules		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	Larry Wall, Tom Christiansen, John Orwant, “Programming PERL”, 2012, Fourth Edition, Oreilly Publications.
2.	John K. Ousterhout, Ken Jones, “Tcl and the Tk Toolkit”, 2010, Second Edition, Pearson Education.
3.	Guido van Rossum Fred L. Drake, Jr., editor, “Python Tutorial Release 3.2.3”, 2012, Python Software Foundation.

Reference Books

1.	Randal L. Schwartz, Brian D Foy, Tom Phoenix, “Learning Perl”, 2021, 8th Edition, O'Reilly Media, Inc.

2.	Mark Lutz, “Learning Python”, 2013, 5th Edition, O'Reilly Media, Inc.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD605L	Advanced Computer Arithmetic	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course is aimed to

1. Introduce the representation of the numbers using redundant and residue number system.
2. Introduce various integer arithmetic algorithms, FFT and modular arithmetic algorithms.
3. Familiarize floating-point arithmetic algorithms and its impacts on resulting error and its corrective methods.
4. Explain CORDIC algorithm for calculating various functions of common interest.
5. Explain the implementation aspects of high throughput, low power and fault tolerant arithmetic circuits.

Course Outcome

At the end of the course students will be able to

1. Interpret and represent the numbers using redundant and residue number system.
2. Apply various integer arithmetic algorithms.
3. Compare and apply various FFT and modular arithmetic algorithms.
4. Classify floating-point arithmetic algorithms, apply it, analyse the impacts of resulting error and its corrective methods.
5. Evaluate CORDIC algorithm for calculating various functions of common interest.
6. Develop high throughput, low power and fault tolerant arithmetic circuits.

Module:1	**Introduction to computer Arithmetic**	**5 hours**
Review of Numbers and arithmetic. Redundant number systems. Residue number system.		
Module:2	**Integer Arithmetic**	**7 hours**
Addition and Subtraction. Multiplication. Division. Roots. Greatest Common Division. Base Conversion: Quadratic Algorithms, Sub quadratic Algorithms.		
Module:3	**FFT and Modular Arithmetic**	**6 hours**
Representation: Classical Representation, Montgomery's Form, Residue Number Systems, MSB vs LSB Algorithms, Link with Polynomials. Addition and Subtration. Multiplication: Barrett's Algorithm, Montgomery's Multiplication, McLaughlin's Algorithm, Special Moduli, Fast Multiplication Over GF (2)[x]. Division and Inversion, Exponentiation, Chinese Remainder Theorem.		
Module:4	**Floating Point Arithmetic**	**7 hours**
Floating point representation. Floating point operation. Errors and Error control. Precise and certifiable arithmetic.		
Module:5	**Function Evaluation**	**7 hours**
Square-Rooting Methods. The CORDIC Algorithms. Variations in Function Evaluation. Arithmetic by Table Lookup.		
Module:6	**Implementations**	**5 hours**
High throughput arithmetic, Low power arithmetic, fault tolerant arithmetic		
Module:7	**Error Analysis**	**6 hours**
Absolute Versus Relative Error, Significant Digits. Uncertainty in Data. Chopping off and Rounding off. Truncation Error. Loss of Significance.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	Behrooz Parhami, “Computer Arithmetic: Algorithms and Hardware Design”, 2015, Second Edition, Oxford University Press.

2.	Richard P Brent and Paul Zimmerman, “Modern Computer Arithmetic”, 2010, Cambridge University Press.		
Reference Books			
1.	Mircea Vladutiu, “Computer Arithmetic: Algorithms and Hardware Implementation”, 2012, Springer.		
2.	Ulrich W. Kulisch “Computer Arithmetic and Validity: Theory, Implementation, and Applications”, 2012, second edition, De Gruyter.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD606L	Mixed Signal IC Design	3	0	0	3
Pre-requisite	MVLD504L	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Introduce the design aspects of dynamic analog circuits and analog-digital interface electronics in CMOS technology.
2. Specify design implementation of ADC & DAC.

Course Outcomes:

At the end of the course the student will be able to

1. Understand the theory of discrete-time signal processing and its implementation using analog techniques.
2. Design Sample and Hold Circuits using MOS by considering the non-idealities.
3. Analyze CMOS based Switched Capacitor Circuits.
4. Understanding basics of Data Converters.
5. Analyze the architectures of ADCs and DAC.
6. Understand the oversampling converter architecture.

Module:1	**Sampling:**	**5 hours**

Introduction – sampling - Spectral properties of sampled signals - Oversampling – Anti-alias filter design. Time Interleaved Sampling - Ping-Pong Sampling System - Analysis of offset and gain errors in Time Interleaved Sample and Hold.

Module:2	**Sampling Circuits**	**5 hours**

Sampling circuits- Distortion due to switch - Charge injection - Thermal noise in sample and holds - Bottom plate sampling - Gate bootstrapped switch -Nakagome charge pump. Characterizing Sample and hold - Choice of input frequency.

Module:3	**Switched Capacitor Circuits:**	**6 hours**

Switched Capacitor (SC) circuits– Parasitic Insensitive Switched Capacitor amplifiers - Non idealities in SC Amplifiers – Finite gain - DC offset - Gain Bandwidth Product. Fully differential SC circuits - DC negative feedback in SC circuits.

Module:4	**A/D and D/A Converters Fundamentals:**	**5 hours**

Data converter fundamentals: Offset and gain Error - Linearity errors - Dynamic Characteristics – SQNR - Quantization noise spectrum.

Module:5	**Analog to Digital Converter Architectures:**	**7 hours**

Flash ADC - Regenerative latch - Preamp offset correction - Preamp Design - necessity of up-front sample and hold for good dynamic performance. Folding ADC - Multiple-Bit Pipeline ADCs and SAR ADC.

Module:6	**Digital to Analog Converter Architectures:**	**7 hours**

DAC spectra and pulse shapes - NRZ vs RZ DACs. DAC Architectures: Binary weighted - Thermometer DAC - Current steering DAC - Current cell design in current steering DAC - Charge Scaling DAC - Pipeline DAC.

Module:7	**Oversampling Converter:**	**8 hours**

Benefits of Oversampling -Oversampling with Noise Shaping - Signal and Noise Transfer Functions - First and Second Order Delta-Sigma Converters. Introduction to Continuous-time Delta Sigma Modulators - time-scaling - inherent antialiasing property - Excess Loop Delay - Influence of Op-amp non idealities - Effect of Op-amp non idealities - finite gain bandwidth - Effect of ADC and DAC non idealities - Effect of Clock jitter.

Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1. Frank Ohnhauser, Analog-Digital Converters for Industrial Applications Including an

	Introduction to Digital-Analog Converters, 2015, First Edition, Springer Publishers.			
2.	David Johns and Ken Martin, Analog Integrated Circuit Design, 2012, Second Edition John Wiley & Sons Inc.			
Reference Books				
1.	Ahmed M.A.Ali, High Speed Data Converters, 2016, First Edition, IET Materials, Circuits & Devices.			
2.	S.Pavan,R. Schreier and Gabor.C.Temes, Understanding Delta – Sigma Data Converters, 2017, First Edition , IEEE Press.			
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test				
Recommended by Board of Studies		28-07-2022		
Approved by Academic Council		No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD607L	RFIC Design	3	0	0	3
Pre-requisite	MVLD504L	Syllabus version			
		1.0			

Course Objectives

The course is aimed to
1. Familiarize with the design of integrated radio frequency front-end circuits.
2. Design RF Power amplifiers and LNA.

Course Outcome

At the end of the course the student will be able to
1. Understand the concepts of RF IC Design.
2. Understand the High Frequency model of MOS and importance of Impedance Matching.
3. Analyze the various transceiver and radio architectures.
4. Design Low Noise amplifiers and Mixers with specifications.
5. Design VCOs and Frequency synthesizers and their applications to transceiver design.
6. Classify and comprehend the design of Power Amplifiers.

Module:1	**Introduction to RF & Wireless Technology:**	**5 hours**
Complexity design and applications - Choice of Technology - Basic concepts in RF Design: Nonlinearly - Time Variance - Intersymbol Interference - random processes - Noise. Definitions of sensitivity - dynamic range -conversion Gain and Distortion.		
Module:2	**High Frequency Model of RF Transistors and Matching Networks:**	**5 hours**
MOSFET behavior at RF frequencies - Noise performance and limitation of devices - Impedance matching networks - transformers and baluns.		
Module:3	**Analog& Digital Modulation for RF Circuits:**	**5 hours**
Coherent and Non coherent detection - Mobile RF Communication systems and basics of Multiple Access techniques - Receiver and Transmitter Architectures and Testing: Heterodyne -Homodyne, Image-reject, Direct-IF and subsampled receivers - Direct Conversion and two steps transmitters.		
Module:4	**Low Noise Amplifiers and Mixers**	**8 hours**
Low Noise Amplifiers: Common Source LNA - Common Gate LNA -Cascode LNA. Mixers: Design of Active and Passive Mixers.		
Module:5	**Voltage Controlled Oscillators and Frequency Synthesizers:**	**8 hours**
Oscillators: Basic topologies VCO and definition of phase noise. Noise-Power trade-off. Resonatorless VCO design - Quadrature and single-sideband generators - Radio Frequency Synthesizers: PLLs.		
Module:6	**RF Power Amplifiers:**	**8 hours**
Class A, AB, B, C amplifiers - Class D, E, F amplifiers - RF Power amplifier design.		
Module:7	**Radio architectures:**	**4 hours**
GSM radio architectures, CDMA, UMTS radio architectures.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	B.Razavi, RF Microelectronics, 2013, Second Edition, Pearson Education Limited.
2.	Hooman Darabi, Radio-Frequency Integrated Circuits and Systems, 2015, First Edition Cambridge University Press.

Reference Books

1.	Gu, Qizheng, RF System Design of Transceivers for Wireless Communications, 2010, Springer.
2.	Bosco Leung, VLSI for Wireless Communication, 2011, Second Edition, Springer.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD608L	VLSI Digital Signal Processing	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Familiarise various representation methods of DSP algorithms, understand the significance of the iteration bound and to calculate the same for a given single-rate and/or multi-rate DFG.
2. Understand and apply the architectural transformation techniques such as retiming, unfolding and folding on a given DFG.
3. Introduce the algorithmic and numerical strength reduction methods for performance improvement.
4. Signify and calculate the effects of scaling and round-off noise for a given digital filter with limited word length.

Course Outcomes:

At the end of the course the student will be able to

1. Compare various representation methods of DSP algorithms.
2. Find iteration bound of a given single and/or multi-rate DFG.
3. Understand and transform the given DFG using retiming with constraints.
4. Apply unfolding and folding transformations on the given DFG.
5. Understand and apply algorithmic and numerical strength reduction methods.
6. Understand and calculate scaling and round-off noise of the given digital filter with limited word length.

Module:1	**Introduction to Digital Signal Processing**	**5 hours**

Typical DSP Algorithms - DSP Application Demands and Scaled CMOS Technologies - Representations of DSP Algorithms - Data-Flow Graph Representations.

Module:2	**Iteration Bound**	**5 hours**

Introduction - Loop Bound and Iteration Bound - Algorithms for Computing Iteration Bound: Longest Path Matrix and Multiple Cycle Mean algorithms - Iteration Bound of Multi-rate Data Flow Graphs.

Module:3	**Pipelining, Parallel processing and Retiming**	**8 hours**

Pipelining and Parallel Processing - Introduction to Retiming - Definitions and Properties - Solving Systems of Inequalities - The Bellman-Ford Algorithm - The Floyd Warshall Algorithm- Retiming Techniques.

Module:4	**Unfolding**	**6 hours**

Introduction, An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding, and Retiming, Applications of Unfolding.

Module:5	**Folding**	**6 hours**

Introduction, Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures.

Module:6	**Algorithmic & Numerical Strength Reduction**	**7 hours**

Introduction to Algorithmic Strength Reduction, Cook-Toom Algorithm, Iterated Convolution, Cyclic Convolution, Discrete Cosine Transform. Introduction to Numerical Strength Reduction, Canonic Signed Digit Arithmetic, Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression Sharing in Digital Filters.

Module:7	**Scaling and Rounding Noise**	**6 hours**

Introduction, Scaling and Rounding Noise, State Variable Description of Digital Filters, Scaling and Rounding Noise Computation, Rounding Noise in Pipelined IIR Filters.

Module:8	**Contemporary Issues**	**2 hours**

	Total Lecture hours:	**45 hours**
Text Book(s)		
1.	Keshab. K.Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, 2014, Reprint, Wiley.	
Reference Books		
1.	John G. Proakis, Dimitris K Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, 2015, Fourth Edition, Prentice Hall.	
2.	Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing, 2014, McGraw-Hill.	
3.	S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, 2010, PHI.	
4.	S. K. Mitra, Digital Signal Processing – A Computer Based Approach, 2010, Fourth Edition, McGraw-Hill.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test		
Recommended by Board of Studies	28-07-2022	
Approved by Academic Council	No. 67	Date 08-08-2022

Course Code	Course Tilte	L	T	P	C
MVLD609L	System-on-Chip Design	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Introducing design, optimization, and programing a modern System-on-a-Chip.
2. Detailing SoC design with on-chip memories and communication networks, I/O interfacing.
3. Making them understand about signal integrity aware SoC design and Scheduling algorithms.

Course Outcomes:

At the end of the course the student will be able to

1. Understand an ability to identify, formulate and treat complex issues in the field of system-on-chip from a holistic perspective.
2. Evaluate the performance of SoC based design by various advanced techniques.
3. Apply System C for system design.
4. Create interconnection structures in a SoC / NoC based system design.
5. Apply static timing analysis for a SoC based design.
6. Analyse the cause and eliminate the issues relevant to signal integrity and scheduling.

Module:1	**Introduction**	**3 hours**
Architecture of the present-day SoC - Design issues of SoC- Hardware-Software Co design – Core Libraries – EDA Tools.		
Module:2	**Design Methodology for Logic, Memory and Analog Cores**	**6 hours**
SoC Design Flow – guidelines for design reuse – Introduction- Efficiency of application specific hardware- Target architectures for HW/SW partitioning -System Integration, Embedded memories – Design methodology for embedded memories – Specification of analog cores.		
Module:3	**Introduction to System C for SoC Design**	**7 hours**
Co-Specification- System Partitioning- Co-simulation, Co-synthesis & Co-verification – SystemC and Co-specification and Co-simulation**.**		
Module:4	**SoC and NoC Interconnection Structures**	**7 hours**
SoC Interconnection Structures- Bus-based Structures- AMBA Bus. Network on Chip -NoC Interconnection Structures-Topologies- routing- flow control- network components (router/switch, network interface, Links).		
Module:5	**STA for SoC Design**	**7 hours**
Timing paths and its Timing Optimization- Slow to High and High to low frequency timing path- Half cycle timing path- Latch time borrowing- Interface Logic Model design and analysis for SoC design.		
Module:6	**Signal Integrity Aware SoC design**	**7 hours**
Signal Integrity overview- EMI (Electro Magnetic Interference) and its protection- ESD and its Protection- Delay- Noise- glitches and its protection- Transmission lines- ringing. Crosstalk and Glitch analysis-Types of Glitches- Glitch Threshold and propagation- Noise Accumulation with Multiple aggressor- Aggressor timing correlation- Crosstalk Delay analysis -Timing Verification using crosstalk delay-Positive and Negative crosstalk-aggressor victim timing correlation- aggressor victim functional correlation.		
Module:7	**Scheduling**	**6 hours**
Introduction and need for HLS- Major steps-Scheduling and Allocation- Binding/Assignment-Concept of Scheduling, Heuristic Scheduling Algorithm**.**		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)			
1.	Michael J. Flynn, Wayne Luk,Computer System Design: System on chip, 2011, First Edition, Wiley-Blackwell.		
2	J. Bhasker, Rakesh Chadha, STA for Nanometer design – A practical approach, 2010, First Edition, Springer.		
Reference Books			
1.	Jose L. Ayala, Communication Architectures for Systems-on-Chip, 2011, First Edition, CRC Press.		
2	Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, System-on-Chip Test Architectures: Nanometer Design for Testability, 2010, First Edition, Morgan Kaufmann.		
3	Ahmed Jerraya and Wayne Wolf, Multiprocessor Systems-on-Chips (Systems on Silicon Series), 2010, First Edition, Morgan Kaufmann.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD610L	Nanoscale Devices and Circuit Design	3	0	0	3
Pre-requisite	MVLD501L	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Understand the CMOS scaling.
2. Design of digital, analog circuits using multigate devices, materials and their properties used for designing Microsensors.
3. Understand the concepts of Microsystem technologies used for realizing Microsensors and actuators.
4. Understand the working principles of Interface Electronic Circuits for resistive, capacitive and temperature sensors.

Course Outcomes:

At the end of the course the students will be able to

1. Understand the CMOS scaling issues
2. Explain the need of novel MOSFET
3. Explain the physics of multigate MOS system
4. Model nanowire FETs.
5. Design digital and analog circuit using multigate devices.
6. Understand the physics of CNTFET

Module:1	**CMOS Scaling Issues and Solutions**	**5 hours**
MOSFET scaling, short channel effects, quantum effects, volume inversion, threshold voltage, channel engineering, source/drain engineering, high-k dielectric, strain engineering, multigate technology mobility, gate stack.		
Module:2	**Introduction to Novel MOSFETs**	**4 hours**
SOI MOSFET, multigate transistors, single gate, double gate, triple gate, surround gate, Silicon Nanowire transistors		
Module:3	**Physics of Multi-gate MOS System**	**6 hours**
MOS electrostatics, 1D, 2D MOS electrostatics, ultimate limits, double gate MOS system, gate voltage effect, semiconductor thickness effect, asymmetry effect, oxide thickness effect , electron tunnel current, two dimensional confinement, scattering.		
Module:4	**Nanowire FETS**	**6 hours**
Silicon nanowire MOSFETs, evaluation of I-V characteristics, I-V characteristics for non-degenerate carrier statistics, I-V characteristics for degenerate carrier statistics, electronic conduction in molecules, general model for ballistic nano transistors, CNT-FETs.		
Module:5	**Digital Circuit Design using Multi-gate Devices**	**7 hours**
Digital circuits design, impact of device performance on digital circuits, leakage performance trade off, multi VT devices and circuits, SRAM design.		
Module:6	**Analog Circuit Design using Multi-gate Devices**	**9 hours**
Analog circuit design, trans-conductance, intrinsic gain, flicker noise, self-heating, band gap voltage reference, operational amplifier, comparator designs, mixed signal, successive approximation DAC, RF circuits		
Module:7	**Carbon Nanotube FET**	**6 hours**
CNT-FET, CNT memories, CNT based switches, logic gates, CNT based RF devices, CNT based RTDs, CNTFET based applications.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1. J P Colinge, FINFETs and other Multi-gate Transistors, 2010, Springer, Germany.

2.	B.G.Park, S.W. Hwang &Y.J.Park, Nanoelectronic Devices, 2012, Pan Stanford Publisher, Singapore.		
Reference Books			
1.	N. Collaert, CMOS Nanoelectronics: Innovative Devices, Architectures and Applications, 2012, Reprint Pan Stanford publisher, Singapore.		
2.	Niraj K. Jha, Deming Chen, Nanoelectronic Circuit Design, 2011, First Edition, Springer London.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD611L	Advanced Computer Architecture	3	0	0	3

Pre-requisite	NIL	Syllabus version
		1.0

Course Objectives

The course is aimed to

1. Introduce advanced concepts of computer architecture.
2. Acquire knowledge on various interconnect topology for multiprocessor system and different pipelining techniques.
3. Understanding different memory hierarchy for multiprocessor and multicomputer systems.

Course Outcome

At the end of the course the student will be able to:

1. Understand the architecture of the various multiprocessors and multicomputer.
2. Identify possible parallel execution at hardware and software level.
3. Determine the required static or dynamic interconnect network for a multiprocessor system.
4. Apply different pipelining techniques to reduce computation time.
5. Analyse the various memory design for multiprocessor and multicomputer.
6. Design scalable parallel architecture for multiprocessor system.

Module:1	**Parallel computer models**	**3 hours**
The state of computing - Classification of parallel computers - Multiprocessors and Multicomputer – Multi-vector and SIMD computers.		
Module:2	**Program and network properties**	**7 hours**
Conditions of parallelism - Data and resource Dependences - Hardware and software parallelism - Program partitioning and scheduling - Grain Size and latency - Program flow mechanisms - Control flow v/s data flow - Data flow Architectures.		
Module:3	**System Interconnect Architectures**	**7 hours**
Network properties and routing - Static interconnection Networks - Dynamic interconnection Networks - Multiprocessor system Interconnects - Hierarchical bus systems - Crossbar switch and multiport memory - Multistage and combining network.		
Module:4	**Pipelining**	**7 hours**
Linear pipeline processor - nonlinear pipeline processor - Instruction pipeline Design - Mechanisms for instruction pipelining - Dynamic instruction scheduling - Branch Handling techniques - branch prediction - Arithmetic Pipeline Design.		
Module:5	**Memory Hierarchy Design**	**6 hours**
Cache basics & cache performance - reducing miss rate and miss penalty - multilevel cache hierarchies - main memory organizations - design of memory hierarchies.		
Module:6	**Shared Memory Architectures**	**7 hours**
Symmetric shared memory architectures - distributed shared memory architectures - cache coherence protocols - scalable cache coherence - directory protocols - memory based directory protocols - cache based directory protocols.		
Module:7	**Multiprocessor Architectures**	**6 hours**
Computational models - An Argument for parallel Architectures - Scalability of Parallel Architectures - Benchmark Performances.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1. Kai Hwang, NareshJotwani, Advanced Computer Architecture: Parallelism, Scalability,

	Programmability, 2011, Second Edition, Tata McGraw Hill Education Pvt. Ltd., India.			
Reference Books				
1.	John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, 2011, Fifth Edition, Morgan Kaufmann.			
2.	DezsoSima, Terence Fountain, Peterr Karsuk, Advanced computer Architectures – A Design Space Approach, 2014, Pearson.			
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.				
Recommended by Board of Studies		28-07-2022		
Approved by Academic Council		No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD612L	Micro Sensors and Interface Electronics	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives :

The course is aimed to:

1. Introduce various types of Microsensors & micro actuators corresponding materials to fabricate it.
2. Make them Understand the concepts of Microsystem technologies used for realizing Microsensors and actuators.
3. Explore the working principles of interface electronics circuits for resistive, capacitive, and temperature sensors.

Course Outcomes :

After the completion of the course, students will be able to:

1. Understand the Micro-Smart Systems and the analysis of MEMS structural design.
2. Analyze the MEMS materials and Properties.
3. Understand the fabrication process flow for Microsystems.
4. Classify and Comprehend different types of Sensors and Actuators.
5. Explain about the wide applications of Microsensors.
6. Understand the basic Interface Circuits.

Module:1	Micro-Smart System and MEMS Structural Analysis	8 hours

Microsystems and scaling law, MEMS &Micro machines, Evolution of Microsystems, Silicon and Non-silicon Micro and Smart Systems. Micro-scale fluid mechanics: Intermolecular forces, States of matter, Continuum assumption, Governing equations, Constitutive relations. Analysis of MEMS structural design: Hooke's law, beam theory, cantilever analysis, plate theory, spring (folded flexure) design, matrix analysis

Module:2	Microsystem Materials and Properties	5 hours

Materials - Silicon, Silicon oxide and nitride, Thin Metal films (Cu, Cr, Au, Ti, Pt, Mo, W), Polymers (SU8,PMMA, PDMS), Glass and Quartz.
Important material properties-Young modulus, Poisson's ratio, density, piezoresistive coefficients, TCR, Thermal Conductivity, Material Structure.

Module:3	Microsystem Fabrication Technology	5 hours

Single Crystal Silicon Growth, Wafer Cleaning, Oxidation, Diffusion, Ion implantation, PVD, CVD, Electroplating, Lithography, Bulk Micromachining, Surface Micromachining, LIGA,Bonding and Packaging.

Module:4	Introduction to Sensors and Actuators	8 hours

Electrostatic, Piezoelectric, Piezoresistive, Electromagnetic, Thermo pneumatic, Shape Memory Alloy, Thermoelectric, Optical: SPR and SERS - Resonant and Micro-channel.

Module:5	Applications of Micro Devices	8 hours

Industrial and Automotive Applications: Pressure Sensors, Accelerometers, Gas Sensors, Flow sensors, Gyroscopes, Micro mixer, Micro Valve, Micro Pump, Micro heater, Ink-Jet printer heads and Micro-mirror TV Projector.
Telecommunication Applications: Imaging and Displays, Fiber optic communication devices. Biomedical Applications: Micro & Nano Cantilevers, Glucose sensors, In-Vitro and In-Vivo Diagnostics. RF Applications – Switches, Phase Shifters, Resonators and Varactors.

Module:6	Interface Circuits	5 hours

Interface circuits for Resistive, Capacitive and Temperature Sensors.

Module:7	Voltage and Current - Mode Approach in Sensor Interfaces Design	4 hours

Voltage-Mode Approach in Sensor Interfaces Design: DC & AC excitation for resistive sensors,capacitive sensor interfacing and temperature sensor interfaces.
Current-Mode Approach in Sensor Interfaces Design: AC-Excitation Voltage for

Resistive/ Capacitive Sensors and DC-Excited Resistive Sensor Interface.				
Module:8	**Contemporary Issues**			**2 hours**
	Total Lecture hours:			**45 hours**
Text Book(s)				
1.	M. Madou, Fundamentals of Microfabrication and Nanotechnology, 2011, Third Edition, CRC Press.			
2.	Anderia De Marcellis, Giuseppe ferri, Analog circuits and systems for voltage-mode and current-mode sensor interfacing applications, 2011, Springer.			
Reference Books				
1.	N. Maluf, K Williams, An Introduction to Microelectromechanical Systems Engineering, 2004, Second Edition, Artech House Inc.			
2.	S. Senturia, Microsystem Design, 2007, Springer Publisher.			
3.	MinhangBao, Analysis and Design Principles of MEMS Devices, 2005, Elsevier Science.			
4.	G. Kovacs, Micromachined Transducers Sourcebook, 1998, McGraw-Hill.			
5.	Kirby, B.J., Micro- and Nanoscale Fluid Mechanics: Transport in Microfluidic Devices, 2010, Cambridge University Press.			
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test				
Recommended by Board of Studies		28-07-2022		
Approved by Academic Council		No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD613L	System Design with FPGA	3	0	0	3
Prerequisite	NIL	Syllabus version			
		1.0			

Course Objectives :

This course is aimed to

1. Provide an overview of FPGA architectures and expound on the softcore and hard-core processors in association with hardware and software co-design.
2. Understand the specification and operation of Programming for peripheral Interfaces and Interconnect Fabrics.
3. Implement digital system and IP blocks for various DSP algorithms.

Course Outcomes :

After completion of the course the student will be able to:

1. Understand and get an idea about SoC and FPGA architectures.
2. Understand the NIOS II soft core processor architecture.
3. Analyze the working of hardware and software co-design flow.
4. Interpret the usage of various peripheral interfaces for system design.
5. Develop a system by choosing suitable interconnect fabrics.
6. Design the system using NIOS II soft core processor, model the system by using IP block and design and develop embedded synthesis using FPGA.

Module:1	**SoC Architecture**	**6 hours**
An Overview of System on Design – FPGA SoC Architecture – Case Study: Xilinx / Intel FPGA		
Module:2	**Soft Core and Hard Core Processor**	**8 hours**
Nios II Processor – Configurability Features – Processor Architecture-Instruction set – ARM cortex A9 architecture		
Module:3	**Hardware – Software Co-design Flow**	**4 hours**
Hardware Design Flow – Software Design Flow - EDA Tool Hardware and Software design flow		
Module:4	**Programming for peripheral Interfaces**	**5 hours**
LCD, PS2, RS232, SDRAM, SRAM Controller, VGA, Audio and Video, PIO, External Bus bridge, and IrDA		
Module:5	**Interconnect Fabrics**	**4 hours**
Avalon Switch Fabric Interconnect - Implementation and Functions- Integrated Design Environment		
Module:6	**System Design**	**8 hours**
Traffic light Controller, Real Time Clock - Interfacing using FPGA: VGA, LCD, Camera		
Module:7	**IP Block Implementation**	**8 hours**
Edge detection algorithm- Image edge detection in FPGA using SOBEL Edge Detection/ Canny Edge Detection Algorithm, Colour and Brightness Enhancement algorithm- Contrast enhancement using RGB to HSV algorithm based on FPGA		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1. ZainalabedinNavabi, “Embedded Core Design with FPGAs”, 2011, TATA McGraw Hill Ltd.
2. Pong P. Chu, Embedded SoPC Design with NIOS II Processor and VERILOG examples”, 2012, Wiley.

Reference Books			
1	Donald G. Bailey," Design for Embedded Image Processing on FPGAs", 2012, Wiley.		
2	Paul J. Deitel, Harvey M. Deitel, "C: How to Program",2012, Pearson Education.		
3	Joseph Yu, System-on-Chip Design with Arm Cortex-M Processors, 2019, ARM Education Media.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD614L	DSP Architectures	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

The course intended to

1. Explore different Digital Signal Processor (DSP) architectures and to design systems using programmable DSPs.
2. Improve system performance using different pipelining techniques, processor array and systolic array.
3. Interface of memory and peripherals to a DSP; and acquire knowledge on different codec implemented on DSP.

Course Outcome

At the end of the course the student will be able to

1. Identify and use specific Digital Signal Processor for various applications.
2. Design a system using programmable DSP.
3. Implement pipelining techniques to improve system performance.
4. Implement applications using processor array and systolic arrays to enhance the performance.
5. Design involving memory and other interfaces to DSP.
6. Design of various codecs on target DSPs.

Module:1	**DSP Integrated Circuits and VLSI Technologies**	**4 hours**
Standard digital signal processors - Application specific IC's for DSP - DSP systems - DSP system design - Integrated circuit design.		
Module:2	**Architectures for programmable DSP**	**6 hours**
Basic Architectural Features - DSP Computational Building Blocks - Bus Architecture and Memory - Data Addressing Capabilities - Address Generation Unit - Programmability and Program Execution - Features for External Interfacing.		
Module:3	**Execution Control and Pipelining**	**6 hours**
Hardware looping – Interrupts – Stacks - Relative Branch support - Pipelining and Performance - Pipeline Depth – Interlocking - Branching effects - Interrupt effects - Pipeline Programming models.		
Module:4	**Synthesis of DSP Architectures**	**8 hours**
Top Down approach to DSP LSI - Circuit Synthesis - High Performance Data Conversion Techniques - LSI Algorithms and Architectures - Hierarchical Design of Processor Arrays - Systolic Arrays - Stack Filters - Wave-front Array Processors.		
Module:5	**Interfacing Memory and I/O to DSP Processors**	**7 hours**
External bus interfacing signals - Memory interface - Parallel I/O interface - Programmed I/O - Interrupts and I/O -Direct memory access (DMA) A Multichannel buffered serial port (McBSP) -McBSP Programming.		
Module:6	**Interfacing CODEC**	**5 hours**
CODEC interface circuit - CODEC programming - A CODEC-DSP interface example.		
Module:7	**Multiprocessor Systems**	**7 hours**
Architectures of Multiprocessors-Performance comparison of -Multiprocessor Structures.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)

1. Lars Wanhammer, DSP Integrated Circuits, 2011, Academic press, New York.

2.	Avtar Singh and S. Srinivasan, Digital Signal Processing, 2012, Thomson Publications.		
Reference Books			
1.	Phil Lapsley, Jeff Bier, Amit Shoham, Edward A. Lee, DSP Processor Fundamentals, Architectures & Features, 2011, First Edition, Wiley-IEEE Press.		
2.	Peter Pirsch, Architectures for Digital signal processing, 2010, Wiley, India.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD615L	Memory Design and Testing	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Expounding the basics and detailed architecture of SRAMs and DRAMs.
2. Model the memory fault and introduce the basic and advanced memory testing patterns.
3. Elaborate the reliability and radiation effect issues of semiconductor memories and present methods for radiation hardening.
4. Review and discuss high performance memory subsystems, advanced memory technologies and contemporary issues

Course Outcomes:

At the end of the course the student should be able to

1. Design SRAMs and DRAMs.
2. Design NVRAMs and Flash Memories.
3. Model memory faults, select suitable testing patterns and develop testing patterns.
4. Incorporate DFT and BIST techniques for semiconductor memory testing.
5. Improve the reliability of semiconductor memories, simulate and model radiation effects and, perform radiation hardening.
6. Contribute to the development of high performance memory subsystems and use advanced memory technologies.

Module:1	Volatile memories	5 hours

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, SOI technology, Advanced SRAM architectures and technologies, soft error failure in SRAM, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM

Module:2	Non-volatile memories	5 hours

Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

Module:3	Memory Testing and Patterns	7 hours

General Fault Modeling – Read Disturb Fault Model – Precharge Faults – False Write Through Data Retention Faults – Decoder Faults. Megabit DRAM Testing Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing Application Specific Memory Testing – Zero/one Pattern – Exhaustive Test Patterns – Walking, Matching and Galloping – Pseudo Random Pattern – CAM pattern.

Module:4	Design For Test and BIST	4 hours

RAM Built-In Self – Test (BIST)-Weak Write Test mode – Bit Line Contact Resistance – PFET Test – Shadow Write and Shadow Read.

Module:5	Reliability and Radiation Effects	7 hours

General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability Design for Reliability Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics.

Module:6	High-Performance Subsystem Memories	7 hours

Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories.

Module:7	Advanced Memory Technologies	8 hours

High-Density Memory Packaging Technologies, Ferroelectric Random Access Memories

(FRAMs)- Analog Memories-Magneto-resistive Random Access Memories (MRAMs)- Experimental Memory Devices Memory Hybrids and MCMs (2D)- Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	A. K.Sharma, Advanced Semiconductor Memories: Architecture, Design and Applications, 2014, John Wiley.
2.	Roberto Gastaldi and Giovanni Campardo In Search of the Next Memory: Inside the Circuitry from the Oldest to the Emerging Non-Volatile Memories, 2017, Springer.
Reference Books	
1.	Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, Advanced Test Methods for SRAMs: Effective Solutions for Dynamic Fault Detection in Nanoscaled Technologies, 2010, Springer,
2.	Hao Yu and YuhaoWang, Design Exploration of Emerging Nano-scale Non-volatile Memory, 2014,Springer.
3.	Takayuki Kawahara (Editor), Hiroyuki Mizuno (Editor), Green Computing with Emerging Memory: Low-Power Computation for Social Innovation, 2012, Springer.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD696J	Study Oriented Project				02
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

1. The student will be able to analyse and interpret published literature for information pertaining to niche areas.
2. Scrutinize technical literature and arrive at conclusions.
3. Use insight and creativity for a better understanding of the domain of interest.

Course Outcome:

1. Retrieve, analyse, and interpret published literature/books providing information related to niche areas/focused domains.
2. Examine technical literature, resolve ambiguity, and develop conclusions.
3. Synthesize knowledge and use insight and creativity to better understand the domain of interest.
4. Publish the findings in the peer reviewed journals / National / International Conferences.

Module Content	(Project duration: One semester)

This is oriented towards reading published literature or books related to niche areas or focussed domains under the guidance of a faculty.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered. Assessment on the project – Report to be submitted, presentation and project reviews – Presentation in the National / International Conference on Science, Engineering Technology.

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD697J	Design Project				02
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

1. Students will be able to design a prototype or process or experiments.
2. Describe and demonstrate the techniques and skills necessary for the project.
3. Acquire knowledge and better understanding of design systems.

Course Outcome:

1. Develop new skills and demonstrate the ability to upgrade a prototype to a design prototype or working model or process or experiments.
2. Utilize the techniques, skills, and modern tools necessary for the project.
3. Synthesize knowledge and use insight and creativity to better understand and improve design systems.
4. Publish the findings in the peer reviewed journals / National / International Conferences.

Module Content	(Project duration: One semester)

Students are expected to develop new skills and demonstrate the ability to develop prototypes to design prototype or working models related to an engineering product or a process.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered. Assessment on the project – Report to be submitted, presentation and project reviews – Presentation in the National / International Conference on Science, Engineering Technology.

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD698J	Internship I/ Dissertation I				10
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

To provide sufficient hands-on learning experience related to the design, development and analysis of suitable product / process so as to enhance the technical skill sets in the chosen field and also to give research orientation.

Course Outcome:

1. Considerably more in-depth knowledge of the major subject/field of study, including deeper insight into current research and development work.
2. The capability to use a holistic view to critically, independently and creatively identify, formulate and deal with complex issues.
3. A consciousness of the ethical aspects of research and development work.
4. Publications in the peer reviewed journals / International Conferences will be an added advantage.

Module Content	(Project duration: one semester)

1. Dissertation may be a theoretical analysis, modeling & simulation, experimentation & analysis, prototype design, fabrication of new equipment, correlation and analysis of data, software development, applied research and any other related activities.
2. Dissertation should be individual work.
3. Carried out inside or outside the university, in any relevant industry or research institution.
4. Publications in the peer reviewed journals / International Conferences will be an added advantage.

Mode of Evaluation: Assessment on the project - Dissertation report to be submitted, presentation, project reviews and Final Oral Viva Examination.

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022

Course Code	Course Title	L	T	P	C
MVLD699J	Internship II/ Dissertation II				12
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

To provide sufficient hands-on learning experience related to the design, development and analysis of suitable product / process so as to enhance the technical skill sets in the chosen field.

Course Outcome:

Upon successful completion of this course students will be able to

1. Formulate specific problem statements for ill-defined real life problems with reasonable assumptions and constraints.
2. Perform literature search and / or patent search in the area of interest.
3. Conduct experiments / Design and Analysis / solution iterations and document the results.
4. Perform error analysis / benchmarking / costing.
5. Synthesize the results and arrive at scientific conclusions / products / solution.
6. Document the results in the form of technical report / presentation.

Module Content **(Project duration: one semester)**

1. Dissertation may be a theoretical analysis, modeling & simulation, experimentation & analysis, prototype design, fabrication of new equipment, correlation and analysis of data, software development, applied research and any other related activities.
2. Dissertation should be individual work.
3. Carried out inside or outside the university, in any relevant industry or research institution.
4. Publications in the peer reviewed journals / International Conferences will be an added advantage.

Mode of Evaluation: Assessment on the project - Dissertation report to be submitted, presentation, project reviews and Final Oral Viva Examination.

Recommended by Board of Studies	28-07-2022		
Approved by Academic Council	No. 67	Date	08-08-2022