VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Electronics Engineering

Department of Micro and Nano Electronics

in association with Entuple Technologies

Cordially invites you for

Two-day Training Program

on

ASIC Design using Cadence EDA Tools

9th – 10th November 2024 (10:00 AM – 5:00 PM)

Venue: Gallery-1 (Shakespeare Gallery)

Who Can Attend

UG and PG Students

Research Scholars

Resource Person

Mr. V. Navaneethakrishnan,
Senior Field Application Engineer,
Entuple Technologies Pvt Ltd., Bangalore

Advisors

Dr. Sivanantham S, Professor & Dean, SENSE

Dr. Jasmin Pemeena Priyadarisini,
Professor & Associate Dean, SENSE

Dr. Jagannadha Naidu K,
Associate Professor, & Head,
Department of Micro & Nano Electronics,
SENSE

Registration Link:

https://events.vit.ac.in/

Registration Fee: Rs. 200 (including GST)

Coordinators

Dr. Antony Xavier Glittas, Asst. Professor Sr.,
Dr. Prayline Rajabai C, Asst. Professor Sr.,
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Agenda

Day-1	Session 1 (10 AM – 1 PM)	Session 2 (2 PM – 5 PM)
Day-1: 9th November 2024	➢ Introduction to IC Physical Design Flow ➢ Cadence EDA tools for PD Flow. ➢ Functional Simulation using Incisive tool. ➢ Coverage analysis using IMC tool ➢ Introduction to TCL Scripting ➢ RTL Synthesis using Genus Synthesis Solution ➢ Physical Aware Synthesis using Genus	➢ Physical Implementation using Innovus that includes ✓ Floor Planning ✓ Power Planning ✓ Placement ✓ CTS ✓ Routing ➢ Timing Analysis including AOCV and POCV ➢ Power Analysis ➢ Parasitic Extraction ➢ ECO flow ➢ DRC, LVS ➢ Generation of GDSII
Day-2	**Session 1 (10 AM – 12 PM)**	**Session 2 (2 PM – 4 PM)**
Day-2: 10th November 2024	➢ Introduction to STA including AOCV and POCV ➢ Timing Analysis using Innovus including AOCV and POCV ➢ STA flow using TEMPUS tool including AOCV and POCV	➢ Introduction to Power Analysis ➢ Power Analysis, IR (Static and Dynamic) and EM analysis using VOLTUS ➢ Basic flow using VOLTUS tool including Power Analysis, IR (Static and Dynamic) and ➢ EM analysis

Demo: The sessions will be demonstrated by using Complex SoC design with 10 minimum macros in the design as an example.