VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Three Days Value Added Program

On

Hands on Training using Cadence Tool for Digital IC Design (VAC 1555)

Department of Micro and Nanoelectronics
School of Electronics Engineering

About the Course: Unlike general-purpose processors found in computers, Application-Specific Integrated Circuits (ASICs) are tailored to perform a single task or a small set of related tasks with high efficiency. This specialization makes them incredibly powerful and energy-efficient for their intended application. Some applications like Cryptocurrency mining, Networking equipment, Consumer Electronics, Automotive Systems etc. A value-added program on (ASICs) could cover a wide range of topics, from fundamental concepts to advanced design techniques.

23rd -March-2025, 30th March 2025 and 31st -March-2025

Time: 8AM to 6PM, Venue: 237A

Highlight of the Course:

- **Basic Introduction to Cadence**
- **Schematic Design Using Cadence Virtuoso and analysis using ADEL**
- **Dynamic CMOS logic Design**
- **Design using Dynamic logic gates**
- **Layout Design – ADEXL and post layout simulation using Assura**
- **Arithmetic Unit – Adder and Multiplier, Memory Design**
- ***E- Certificate will be provided.***

Target Audience: **UG/PG students & Research Scholars**

Payment Link : https://events.vit.ac.in/

- **Registration Fee:** Rs 500+ 18% GST.

Course Experts

Dr. Harish M Kittur

Dr. Ravi S, SENSE

Dr. Debashish dash, SENSE

Dr. Satheesh Kumar, SENSE

Dr. Rajeev Pankaj Nelapati, SENSE

Seats Limited to 50 Participants

Advisory Committee

Dr. Jasmin Pemeena Priyadarisini M,

Higher Academic Grade & Dean, School of Electronics Engineering (SENSE)

Dr. Jagannadha Naidu K,

HoD- Dept of Micro and Nanoelectronics, SENSE

Faculty Coordinators:

- ✓ **Dr. S Ravi, SENSE M: 9790155650**
- ✓ **Dr. Debashish Dash M: 8249355210**
- ✓ **Dr. Satheesh Kumar M: 8124424714**
- ✓ **Dr. Rajeev Pankaj Nelapati, M: 9043266364**