VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)
40 YEARS OF TRANSFORMING LIVES

Three-day National Workshop on

ASIC Design using Synopsys EDA Tools

April 25-27, 2025

Organized by

School of Electronics Engineering
Vellore Institute of Technology, Vellore
Tamil Nadu, India

VIT-Technology Business Incubator

Ministry of Electronics and Information Technology
Government of India

MeitY Startup Hub
Delivering Innovation!

VLSI Society of India

INSTITUTION'S INNOVATION COUNCIL
(Ministry of Education Initiative)

About the workshop

The ASIC Design workshop primarily focuses on providing comprehensive hands-on experience in ASIC design and physical verification using Synopsys EDA tools and extensive lab practice. By the end of the course, participants will have a thorough understanding of the complete ASIC design flow, which includes synthesis, partitioning, floor planning, power planning, timing analysis, clock tree synthesis, and routing of functional unit blocks, as well as physical verification and sign-off checks. This workshop also assists faculty in guiding students as they work towards chip design for fabrication.

This workshop is supported by the VIT's Technology Business Incubator (VIT-TBI) and the Ministry of Electronics and Information Technology (MeitY), Government of India and Technically Co-sponsored by VLSI Society of India – Tamil Nadu Chapter.

Registration

A registration fee of Rs. 500/- per participant (inclusive of 18% GST)

Registration Link: https://events.vit.ac.in/

Last date for registration: 12th April 2025

The registration fee includes a Registration Kit, Working Lunch and refreshments for three days, and a certificate.

Participants must make their own arrangements for their accommodations.

Total number of participants: 50

Program Coordinators

Prof. Sivanantham S
Professor,
Group Coordinator, VLSI Society of India – Tamil Nadu Chapter
Email: ssivanantham@vit.ac.in
Mobile: 9894432359

Prof. Jagannadha Naidu K
Associate Professor and HoD,
Micro and Nanoelectroncis
Email: jagannadhanaidu.k@vit.ac.in
Mobile: 9943062343

Contents

ASIC Design Flow
Basics of STA, Standard Cell library
Logic Synthesis and Constraints
DFT Synthesis
Physical Design – Floor planning, Placement
Physical Design – CTS, Routing
Physical Design Verification
Lab on Logic Synthesis & STA
Lab on DFT Based Synthesis
Lab on Floor planning, Placement
Lab on CTS, Routing
Lab on Physical Design Verification

Outcome of the Workshop

The trained faculty members are expected to teach and train their students in the upcoming semester.

Course materials and a lab database will be provided to the faculty.

Who can attend?

- ✓ Faculty members from engineering institutions who teach VLSI courses as part of their undergraduate or postgraduate curriculum.
- ✓ A maximum of two faculty members from each institution.