National workshop
on
"HANDS ON FPGA: FROM BASIC LOGIC TO REAL-WORLD APPLICATIONS"

(HYBRID MODE)

28th & 29th August 2025

Organized by

VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Department of Micro and Nano Electronics
School of Electronics Engineering (SENSE)
Vellore Institute of Technology (VIT)
Vellore-632014

The aim of the program

- Exposure to FPGA Design flow Using AMD Vivado ML Edition
- Exposure IP IP-based design flow
- Exposure to the implementation of Embedded systems using an FPGA

Who Can Attend?

- Faculty, Research scholars, PG and UG students.

Course Content:

- Introduction to Xilinx 7 series FPGA Architecture and families
- Introduction to Vivado Design flow
- Elaboration and Simulation
- IP-based design flow example
- Interfacing PMODS with FPGA
- Implementation on Nexys and Basys kits
- Introduction to Embedded system design using ZYNQ
- Designing with IP integrator
- Extending embedded system into Programmable logic
- Implementation on Nexys and ZCU104 using Vivado ML edition, Vitis Ide, Tera Term

Venue: TT727, SENSE, VIT, Vellore

Registration fee:

- Internal Participants: Rs 500/- (Including GST)
- External Participants: Rs 1000/- (Including GST

Chairperson:
Dr. Jasmine Pemeena Priyadarshini
Professor & DEAN, SENSE

Convenor:

Dr. K. Jagannadha Naidu
HOD, MNE, SENSE

Coordinators

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Resource Persons:

Experts from Corel Technologies

Last date for Registration:
On or before: 27th August, 2025

Registration Link:
Visit: https://events.vit.ac.in/