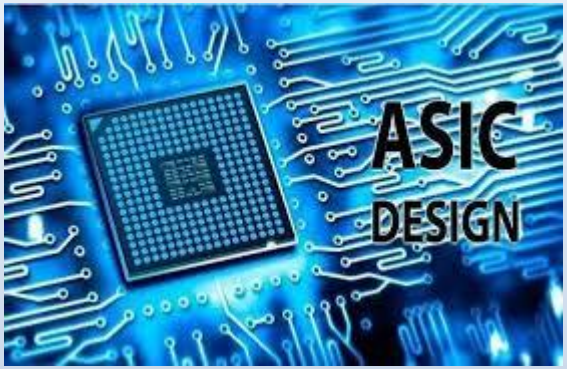
VIT
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Faculty Development Program
on

Hands on ASIC Design using Cadence Tools

(Hybrid Mode)

27th June – 29th June, 2025



Organized by

Department of
Micro & Nanoelectronics,
School of Electronics Engineering,
VIT, Vellore-632014

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About The Institute

VIT Vellore was established with the aim of providing higher quality education at par with international standards. It persistently seeks and adopts innovative methods to improve the quality of higher education on a consistent basis. The campus has a cosmopolitan atmosphere with students from all corners of the globe. Experienced and learned teachers are strongly encouraged to nurture the students. The global standards set at VIT in the field of teaching and research spur us on in our relentless pursuit of excellence.

Our Memoranda of Understanding with various international universities are our major strength. They provide for an exchange of students and faculty and encourage joint research projects for the mutual benefit of these universities. VIT Vellore is the first Indian Institute to get International Accreditation from IET and EI, UK. VIT Vellore obtained the highest possible grade of "A++" from NAAC during the re-accreditation process in 2024. VIT ranked No.1 private engineering institute by MHRD [NIRF-2024 ranking]. With steady steps, we continue our march forward. We look forward to meeting you here in VIT.

About the School of Electronics Engineering

School of Electronics Engineering (SENSE) has more than 170 faculty members who have done their Ph.D degrees from the top-notch universities. The faculty of the SENSE engage in cutting-edge technology teaching and research in fields such as: Wireless communication and Networking, Signal processing, Microwave Imaging, Antenna design, MEMS and Microstructures, Free space optical communication, Robotics and automation, Computer vision and machine learning, Sensors and IoT, Sensors, Automotive sensors, Biomedical Instrumentation, Flexible and wearable electronics, Heterogeneous computing, RTOS and Embedded systems, Analog and Digital IC design, System design with FPGA, and reversible data hiding.

The School has many industry sponsored advanced laboratories for doing research. The School has signed MoUs with many foreign Universities, research organizations and Industries from where students get benefits for their R&D Work / Projects from the MoUs. The School is actively involved in R&D activities and has sponsored projects from various agencies like DRDO, DST, ISRO (RESPOND), and BRNS.

About The Workshop

The primary objective of a three-day Faculty Development Program (FDP) on ASIC Design using Cadence tools is to enhance the knowledge and practical skills of faculty members in the domain of VLSI design, specifically targeting the ASIC design flow using industry-standard Electronic Design Automation (EDA) tools. The program offers a comprehensive overview of the complete ASIC design flow—from Register Transfer Level (RTL) design and simulation to synthesis, Design for Testability (DFT), and physical design implementation. Participants gain in-depth exposure to Verilog HDL, focusing on writing synthesizable code for both combinational and sequential circuits, and learn the nuances of RTL design and its translation to gate-level implementations. A significant highlight of the FDP will be the hands-on lab sessions using Cadence design tools, including ICFB, NC Launch, Genus, Modus, Innovus, and LEC. These sessions enable participants to practically implement concepts such as FSM design, synthesis, timing analysis, logic equivalence checking, DFT, and signal integrity-aware physical design.

Registration Fees:

For Faculties:

External members: **Rs. 1180/-**
(Inclusive of GST)

Internal members: **Rs. 890/-**
(Inclusive of GST)

Important Dates:

Last date for registration: **25th June, 2025**
Workshop Date: 27**th June, 2025**

Please register through the link below:
https://events.vit.ac.in/

Lecture Topics

- **ASIC Design Flow**
- **Verilog HDL for Combinational circuits**
- **Verilog HDL for Sequential circuits**
- **Synthesizable RTL**
- **FSM Design**
- **Simulation Using Cadence NC Launch**
- **RTL Design Flow**
- **Gate level Simulation**
- **DFT Flow**
- **RTL Synthesis Using Cadence genus**
- **Advanced Synthesis**
- **Timing Analysis, DTA**
- **Static Timing Analysis (STA)**
- **Conformal Smart Logic Equivalence Checker (LEC)**
- **DFT Using Cadence Modus**
- **Physical Design Using Cadence Innovus**