VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

10 Days Summer Internship

ON

DIGITAL HARDWARE ARCHITECTURE DESIGN: VERILOG, PIPELINE PROCESSORS & FPGA IMPLEMENTATION

Date: 16th to 26th June, 2025

(Hybrid Mode)

Organizers

Dr. Vikas Vijayvargiya
Associate Professor, VIT Vellore
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Dr. Naushad Manzoor Laskar
Assistant Professor, VIT Vellore
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- E-Certificates will be provided to participants
- No TA/DA/Accommodation will be provided
- For more details, please contact the organizers

Organized by:

Department of Micro and Nanoelectronics
School of Electronics Engineering
VIT, Vellore

Advisors

Dr. Jasmin Pemeena Priyadarisini
Dean, SENSE, VIT Vellore

Dr. Sakthivel R
Associate Dean, SENSE

Dr. Sri Adibhatla Sridevi
HOD, Dept. of MNE, SENSE, VIT Vellore

Target Participants:
UG/PG/PHD Scholars

Registration Fees:
Rs. 300/- (Internal Participants)
Rs. 500/- (External Participants)
(Excluding 18% GST)

Registration Link:
https://events.vit.ac.in/