One Day workshop on

On

ASIC Design Using Cadence Tools

Department of Micro and Nano electronics engineering
School of Electronics Engineering , VIT , Vellore.

About the Course: The *Value-Added Lecture on ASIC Design* aims to introduce students to the most in-demand skills in the field of ASIC design. The course covers both the fundamental concepts and practical hands-on training required in ASIC development. Students will gain experience across the complete design flow — from RTL to Netlist generation — including timing design using **Tempus** and DFT implementation using the **Modus** tool. This comprehensive training enables students to efficiently manage design projects and build a strong foundation for a career as an **ASIC Design Engineer**

Highlight of the Course:

- 8 hours Course Duration
- Introduction to Timing and DFT
- Practical training: Hands on experience
- STA using Cadence TEMPUS
- DFT Using Cadence MODUS

Contact Numbers
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9894972399 – Karthikeyan – TO
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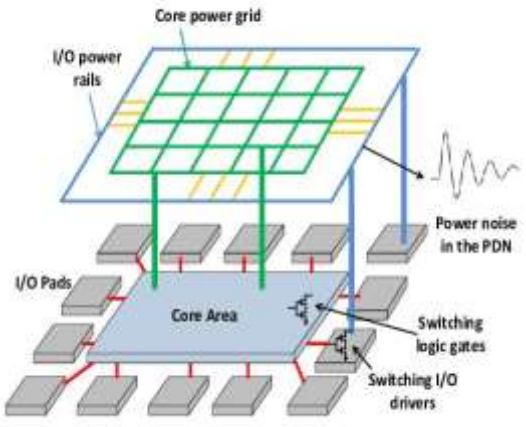
Registration amount : Rs 200/ (Incl of GST)

Date : 01-11-2025
Time : 9am to 5pm

Course Experts

Industry: Mr. Navaneetha Krishnan Veerachamy, Senior Field Application Engineer at Entuple Technologies in Bengaluru, India.

Faculty: Dr. Harish M Kittur. Dr Ravi S SENSE



Advisory Committee

Dr. Jasmin Pemeena Priyadarisini
Dean, School of Electronics Engineering,VIT,Vellore

Dr. Sri Adibhatla Sridevi,
Professor & HOD
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