About the Institution

VIT was established with the aim of providing quality higher education on par with international standards. The global standards set at VIT in the field of teaching and research spur us on in our relentless pursuit of excellence. In fact, it has become a way of life for us. The highly motivated youngsters on the campus are a constant source of pride. Many of our students, who pursue their research projects in foreign universities, bring high quality to their work and esteem to India and have done us proud. With steady steps, we continue our march forward. We look forward to meeting you here at VIT.

About the SCHOOL OF ELECTRONICS (SENSE) School

SENSE at VIT was established for imparting state-of-the-art knowledge in Electronics and Communication Engineering, VLSI and allied areas. B.Tech. Electronics and Communication Engineering is accredited by the Engineering Accreditation Commission of ABET, http://www.abet.org. Faculty are actively involved in R&D activities and are working on research projects funded by government organizations like DRDO, ISRO (RESPOND), BRNS and agencies like DST.

About the Micro and Nano Electronics (MNE) Department

MNE students are in great demand in various core companies like Intel, Texas Instruments, Cadence, ARM, Open Silicon, ST Microelectronics, MediaTek, Qualcomn, Synopsis, Xilinx, NXP Semiconductors etc

Chief patron

Dr. G.Viswanathan, Chancellor, VIT, Vellore

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Dr. Sriadibhatla Sridevi, Professor & HoD - MNE

Coordinators

Dr. Ravi S, Associate Professor

Dr. Sakthivel Ramachandran , Professor Associate Dean, SENSE.

(Registration Limited to 50 Participants on First come First Serve Basis)

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For Internal s

No Rag Fees for Internal Faculty & RA : Use VTOP , TLCE , VIT portal

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For Externals

For Registration use the following link https://events.vit.ac.in/

Registration Fee - Rs 3500 /- (Incl GST)

Accommodation :

Note : Participants need to arrange their own accommodation.

Working Lunch will be provided to externals

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VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING
In Association with
Teaching Learning Centre of Excellence (TLCE)
Invites you for the

Faculty Development Program on

"System on Chip Design: From basics to applications"

Dates: 1st – 5th December 2025

COORDINATORS

Dr. Ravi S

Dr. Sakthivel Ramachandran

Organized by

Department of Micro and Nano electronics (MNE)

School of Electronics Engineering (SENSE)

Vellore Institute of Technology (VIT)

Vellore-632014

Topics

Day 1
Inauguration / Importance of FDP
Importance of FDP
Transistors to Tapeout
Fab For Academics
Complete FPGA Design Flow
FPGA based system design (Hands on)
Day 2
Development of SoC for Industrial applications
Development of SoC for Industrial applications
Development of SoC for Industrial applications
Day 3
ASIC Design - Introduction
STA, Standard cell Lib and RTL synthesis
Hands on RTL Synthesis ,Gate level Simulation & Logic Equivalence Check
Day 4
DFT for Nanometer Design
Hands On DFT
Physical Design Flow
Day 5
Hands on Physical Design
Hands on Physical Design- DRC, LVS
Mini Project Implementation by participants

Objectives of the Programme

SoC (System on a Chip) design is the process of creating a single integrated circuit that integrates most or all components of a computer or electronic system, including the processor, memory, and input/output peripherals. The design process involves defining the architecture, selecting and assembling pre-verified intellectual property (IP) blocks, and ensuring seamless integration to achieve the required functionality, performance, and power efficiency.

Resource Persons

Dr. Kanchana Baskaran ,Vice Chancellor,VIT,Vellore.
Dr. Harish M Kittur , Professor , VIT.
Mr Padmanaban , Intel , Bangalore
Dr. R.Sakthivel , Asso Dean,SENSE ,VIT.
Dr.Kumaravel S
Dr. Sivanatham S
Dr . Sriadibhatla Sridevi. HOD-MNE, VIT.
Dr. Nithish Kumar V
Dr. JagannadhaNaidu,
Dr. Rajeev pankaj Nelapati
Dr. Ragunath G
Dr. Ravi S

Session Mode and requirements

Mode : OFFLINE MODE

No of Sessions : 20

Attendance : 80% is mandatory

Eligibility

This FDP is open to UG, PG, RA scholars, and faculty members of AICTE-approved institutions, as well as industry professionals

Prerequisite

Digital Logic design

Key date

Last Date for registration and payment : 29/11/2025

For Further details Contact

FDP Coordinators

Dr.Ravi S - 9790155650
Dr.Sakthivel Ramachandran – 9994627570

E-mail : msravi@vit.ac.in ; rsakthivel@vit.ac.in