

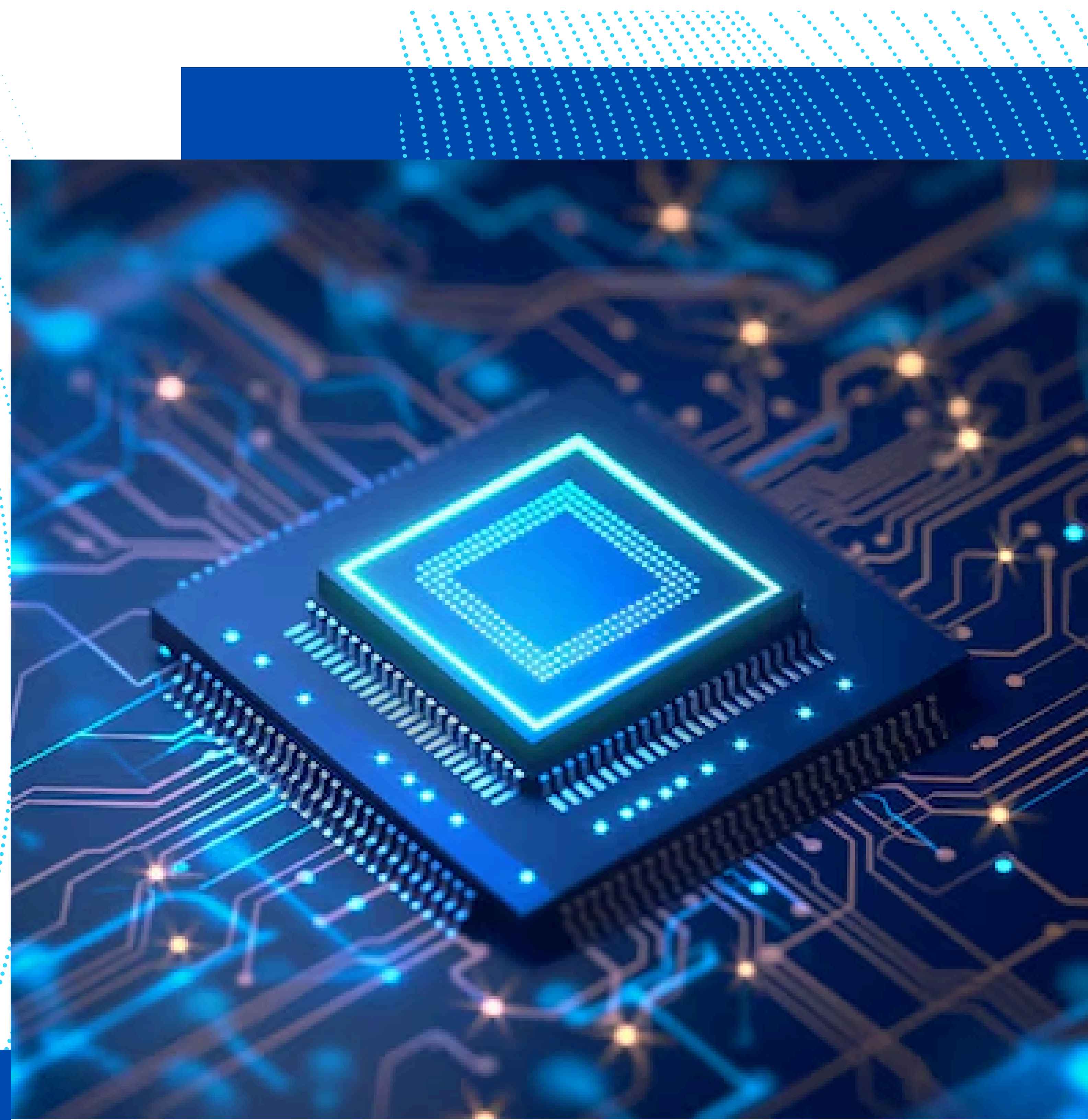
**VIT**Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

VALUE ADDED COURSE

Implementation of ML Algorithms with FPGA - VAC2515

Organized By:
School of Electronics Engineering (SENSE)

 07 Feb - 04 April, 2025



About the Course

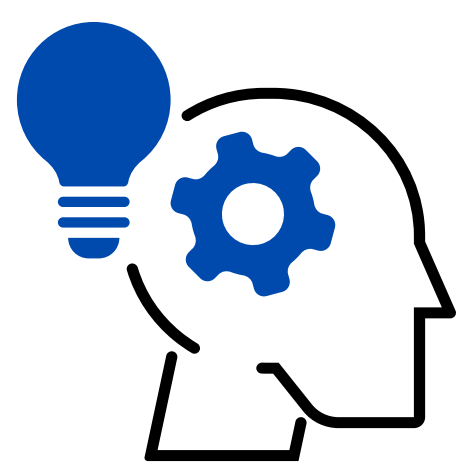
The value-added course, "Implementation of Machine Learning Algorithms with FPGA," aims to familiarize students with ML models for edge computing, the need for hardware acceleration, and the practical implementation of ML, NN, and DNN algorithms on FPGA platforms. The course includes hands-on sessions with FPGA design tools, HLS-based acceleration, optimization techniques such as quantization and pruning, and deployment workflows for real-time ML applications.



Advisory Committee

Dr. Jasmine Pemeena Priyadarsini,
Dean, SENSE

Dr. R.Sakthivel
Associate Dean, SENSE



Resource Persons

Mr. Padmanaban Kalyanaraman
Intel, Bangalore
and

Subject Experts
Dept. of MNE,SENSE



Faculty Coordinators

Dr. S. Sridevi
sridevi@vit.ac.in

Dr. Prachi Sharma
prachi.sharma@vit.ac.in

Dr. Rajeev Pankaj Nelapati
rajeevpankaj@vit.ac.in

Highlights

- ✓ 30 Hours Training
- ✓ ML, NN, DNN, CNN Overview
- ✓ FPGA Design Basics & HLS Tools
- ✓ ML on FPGA: Regression, SVM, DT, RF
- ✓ Neural Networks & CNN Acceleration
- ✓ Optimization: Quantization, Pruning
- ✓ Case Study: CNN + OpenCV Use Cases
- ✓ Hands-on training using DE1-SoC board, Google Colab, Quartus Prime
- ✓ E-Certificate (75% attendance + 60% marks)



Schedule

07.02.26 | 9 AM – 1 PM
 08.02.26 | 9 AM – 1 PM
 15.02.26 | 9 AM – 1 PM
 21.02.26 | 9 AM – 1 PM
 22.02.26 | 9 AM – 1 PM
 08.03.26 | 9 AM – 1 PM
 29.03.26 | 9 AM – 1 PM
 04.04.26 | 9 AM – 1 PM



Seats Limited to 60 Participants



Registration

Fee: ₹500 (GST Included)



Link: <https://events.vit.ac.in/>



Contact

9315043596 - Dr. Prachi Sharma

9043266364 - Dr. Rajeev Pankaj Nelapati

 Venue: TT-312, VIT Vellore