VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

School of Electronics Engineering (SENSE)

Department of Micro & Nano Electronics

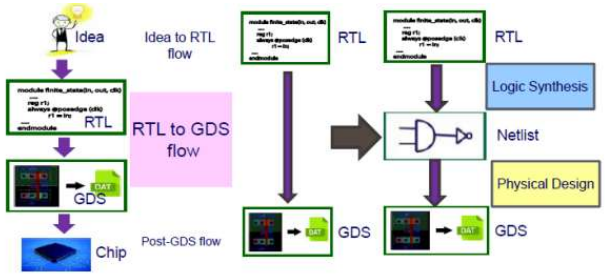
Offers

Value Added Course

on

VAC2336 RTL to GDSII

(SYSTEM ON A CHIP DESIGN)



7th February to 4th April 2026

About VAC:

With today's increasingly large and complex digital IC and system-on-chip (SoC) designs, design power closure, circuit power integrity and Testing become one of the main engineering challenges, thereby impacting the device's total time-to-market. This VAC will teach you how to implement a design from RTL-to-GDSII using various industry standard tools. You will start by coding a design in Verilog, simulate, synthesize, optimize and PnR for a better design.

Who Can Attend?

➔ VIT Students –UG/PG [B.Tech (VLSI) and M.Tech (VLSI Design) students are exempted].

Key Benefits:

This course is designed to introduce the engineers to the area of specification to chip design. The candidates who successfully undergo this training would be able to design a digital system optimized in terms of area, power and timing by applying appropriate constraints. It enable them to apply all possible Power minimization and DFT techniques to build a more reliable system. It provides them an opportunity to carry out the industry standard projects from specification to GDSII.

Last date for Registration:

On or before : 18th January 2026

Course Fee:

Registration Fee: VIT Student: **Rs.500/-**
(Inclusive of GST)

Course Material and projects will be provided to all.

Certificate will be issued for those students who have 75% attendance and 50% Marks in the evaluation)

Course Content:

- FSM Coding Guideline and Coding Style for Synthesis
- Architecture of Logic Synthesizer
- Synthesis Optimization- Timing Parameter Definition – Setup and Hold Timing Check
- Multicycle Paths- Half-Cycle Paths- False Paths.
- Low Power Synthesis, DFT Based Synthesis.
- Pattern Generation- Fault Simulation – Scan Chain Insertion- Fault Coverage.
- Floor plan, Placement, CTS and routing– ECO flow – Signal Integrity Issues,
- Timing Sign-off, Physical Verification
- Mini Project.

Convener:

Dr. Jasmin Pemeena Priyadarsini M
Dean, School of Electronics (SENSE)

Co-Convener:

Dr. Sriadibhatla Sridevi

HoD, Department of Micro & Nano Electronics

Coordinators:

➔ **Dr. Sakthivel Ramachandran**
Professor

➔ **Dr. Jagannadha Naidu K**
Associate Professor

➔ **Dr. Ragunath G**
Assistant Professor

For Registration contact:

Mr.V.Karthikeyan
Contact No.: 9894972399

Event Venue:

TT238, Technology Tower

Online Payment link

Link: https://events.vit.ac.in

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SCHEDULE FOR VAC (32 hours)

Date	Timing	Topics & Faculty
Saturday 7/02/2026	9.30AM-11AM	Coding Style for Synthesis- Dr. Ragunath G
	11.15AM-12.30PM	FSM Coding Guideline- Dr. Ragunath G
	2.30PM-3.30PM	Architecture of Logic Synthesizer, Basics of STA- Prof.Jagan
8/02/2026 Sunday	9.30AM-11AM	Basics of Testing Pattern Generation- Fault Simulation &FC, Prof.Sakthivel
	11.15AM-12.30PM	DFT Based Synthesis, LBIST & MBIST- Prof.Sakthivel
	2.30PM-3.30PM	Lab for Logic Synthesis & STA - Dr. Ragunath G &Dr. Sakthivel, Prof. Jagan
15/02/2026 Sunday	9.30AM-11AM	Lab for Power optimization at Logic Synthesis- Prof.Jagan
	11.15AM-12.30PM	GLS and LEC- Dr. Ragunath G
	2.30PM-3.30PM	Mini Project Spec discussion for implementation- Prof.Jagan, Dr. Ragunath G &Dr. Sakthivel
21/02/2026 Saturday	9.30AM-11AM	Lab: Combinational circuit, Test pattern generation, FC etc- Dr. Sakthivel
	11AM-12.30PM	Lab: DFT Synthesis, scan chain insertion and analysis- Dr. Sakthivel
	2.30AM-3.30PM	PD- Floor plan- Prof.Jagan
22/02/2026 Sunday	9.30AM-11AM	PD- Placement, CTS and routing- Prof.Jagan
	11AM-12.30PM	PD- Placement, CTS and routing- Prof.Jagan
	2.30AM-3.30PM	ECO flow – Signal Integrity Issues- Prof.Jagan
08/03/2026 Sunday	9.30AM-11AM	PD Lab- Prof.Jagan & Dr. Ragunath G
	11AM-12.30PM	PD Lab- Prof.Jagan & Dr. Ragunath G
	2.30AM-3.30PM	PD Lab- Prof.Jagan & Dr. Ragunath G
29/03/2026 Sunday	9.30AM-11AM	Industry Expert Lecture
	11AM-12.30PM	Industry Expert Lecture
	2.30AM-3.30PM	Mini Project implementation and discussion
04/04/2026 Saturday	9.30AM-11AM	Mini Project Evaluation and Exam- Prof.Jagan &R. Sakthivel, Dr. Ragunath G
	11AM-12.30PM	Mini Project Evaluation- Prof.Jagan & Dr.Sakthivel
	2.30AM-3.30PM	Feedback & closing ceremony