VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING

M. Tech VLSI Design

(M.Tech MVD)

Curriculum

(*2025-2026 admitted students*)

VIT®

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(Deemed to be University under section 3 of UGC Act, 1956)

Adaptive Curriculum for Excellence –ACE 2025-26

M.Tech VLSI Design

Program Educational Objectives

1. The graduates will be successful in setting their career paths as VLSI design, test and verification engineers in the industry as well as researchers in the relevant fields.

2. The students will be engineering practitioners and leaders, who would help in addressing the challenges in the semiconductor industry.

3. The graduates will be able to function in their profession as VLSI engineers with social awareness and responsibility and contribute to the economic growth of the country.

Program Outcomes

PO1: An ability to independently carry out research or investigation and development work to solve practical problems.

PO2: An ability to write and present a substantial technical report/document.

PO3: Students should be able to demonstrate a degree of mastery over the area as per the specialization of the program.

PO4: Apply advanced concepts in Physics of semiconductor devices to design VLSI systems.

PO5: Design ASIC and FPGA based systems using industry standard tools.

PO6: Solve research gaps and provide solutions to socio-economic, and environmental problems.

Curriculum Structure

Program Credit Structure	Credits
University Core Courses	39
Professional Core Courses	24
Professional Elective courses	14
Open Elective Courses	03
Total Graded Credit Requirement	**80**

University Core courses (39 Credits)

S.No	Course Title	L	T	P	C
1	Technical Report Writing	1	0	4	3
2	Qualitative and Quantitative Skills Practice I	3	0	0	3
3	Qualitative and Quantitative Skills Practice II	3	0	0	3
4	Project Work	0	0	0	10
5	Internship I/ Dissertation I	0	0	0	10
6	Internship II/ Dissertation II	0	0	0	10
	Total Credits				**39**

Professional Core courses (24 Credits)

S. No	Name of the Course	L	T	P	C
1	VLSI Devices and Technology	3	0	2	4
2	Digital IC Design	3	1	0	4
3	Digital System Design with FPGA	3	0	2	4
4	Analog IC Design	3	0	2	4
5	ASIC Design	3	0	2	4
6	VLSI Testing and Testability	3	0	2	4
	Total Credits				24

Professional Elective courses (14 Credits)

S. No	Name of the Course	L	T	P	C
7	Low Power IC Design	3	0	0	3
8	VLSI Verification Methodologies	3	0	2	4
9	Mixed signal IC Design	3	0	0	3
10	CAD for VLSI	3	1	0	4

11	**System-on-Chip Design**	**3**	**1**	**0**	**4**
12	**Nano Scale Devices and Circuit Design**	**3**	**0**	**0**	**3**
13	**RF IC Design**	**3**	**0**	**0**	**3**
14	**Advanced Computer Architecture**	**3**	**0**	**0**	**3**
15	**Neuromorphic computing**	**3**	**0**	**0**	**3**
16	**VLSI Digital Signal Processing**	**3**	**0**	**0**	**3**
17	**Electromagnetic Interference and Compatibility**	**3**	**0**	**0**	**3**
18	**Embedded System Design**	**3**	**1**	**0**	**4**
19	**Machine Learning and Deep Learning**	**3**	**1**	**0**	**4**

Course Code	VLSI Devices and Technology	L	T	P	C
MAVLD xxxx		3	0	2	4
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

1. Elucidate the fundamentals of intrinsic and extrinsic semiconductors, including carrier concentration, modeling, and the physics of various carrier current transport and tunneling mechanisms.
2. Understand the detailed physics and modelling of PN junction, MOS Capacitors, MOSFET
3.Understand the process involved in semiconductor manufacturing and fabrication

Course Outcomes

1. Apply semiconductor physics & band diagrams to the design of PN junctions
2. Simulate and analyze the MOSCAP and MOSFET device structures.
3. Employ the VLSI fabrication processes for the manufacture of integrated circuits
4. Apply thin film deposition techniques for VLSI fabrication process
5. Design of VLSI devices using TCAD tools

Module:1	Semiconductor Physics and devices	15 hours

Introduction to semiconductor physics-Energy band diagrams-space charge layers-Poisson equation-Electric fields and potentials-p-n junction under applied bias-static current-voltage characteristics of p-n junctions-Breakdown mechanisms, p-n junction capacitance. Metal Gate-semiconductor work function, Energy band diagram of Metal-Oxide-Semiconductor contacts, Mode of Operations: Accumulation, Depletion, midgap and Inversion, 1D Electrostatics of MOS, Depletion Approximation, C-V characteristics of MOS, LFCV and HFCV, Non-idealities in MOS, oxide fixed charges, interfacial charges, flat band voltage, threshold voltage, MOSFET characteristics-triode, saturation region, channel length modulation.

Module:2	Device Modeling using TCAD	7 hours

Introduction to Technology computer aided design (TCAD) tools; Device simulation-terminal characteristics and distributions of carriers, current, field, potential and energy band diagrams within the device, Process simulation-observation of device structure and doping profile.

Module:3	IC Fabrication	8 hours

Introduction to semiconductor Manufacturing and Fabrication, Overview of lithography: Photo-, e-beam, Deep UV and nano-imprint lithography and their limitations, Oxidation, Nitridation, Technological challenges, Dry etching, wet etching.

Module:4	Diffusion and Ion Implantation	7 hours

The diffusion process, Mathematical model for diffusion, The diffusion coefficient, successive diffusions, Diffusion systems, implantation technology, Mathematical model for ion implantation, selective implantation, Channeling, Lattice damage and annealing, Shallow implantations, doping challenges for 3D device structures.

Module:5	Thin Film Deposition	6 hours

Thermal evaporation, e-beam evaporation, DC & RF sputtering, Chemical vapour deposition (Thermal, Plasma enhanced, metal organic), Electrodeposition, Molecular beam epitaxy, Atomic layer deposition

Module 6	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours

Text Books

1	S.M.Sze, M.K.Lee, Semiconductor Physics And Devices, 3ed, An Indian Adaptation, Wiley India, 2021.

2	Plummer James D, Silicon VLSI technology: fundamentals, practice and modeling. 1st edition, Pearson Education India, 2009.
3	J. P. Colinge, C. A. Colinge, Physics of Semiconductor Devices, Springer New York, NY, 2002.
Reference Books	
1.	Yaguang Lian, Semiconductor Microchips and Fabrication: A Practical Guide to Theory and Manufacturing,Wiley-IEEE, 2022
2.	C.Hu, Modern Semiconductor Devices for Integrated Circuits, Pearson, 2009.
3.	S.M.Sze,M-K.Lee, Semiconductor Devices, Physics and Technology, 8th edition, Wiley,2015.
4.	Richard C. Jaeger, Introduction to Microelectronic Fabrication: Volume V: 5 (Modular Series on Solid State Devices, Vol 5), Pearson,1988
Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT	

List of Experiments (Indicative)

Indicative Experiments		**Total Hours**
1.	Introduction to TCAD tools	**2 hours**
2.	Energy Band Diagram and Carrier Concentration Analysis in P-N Junctions • Simulate energy band bending under equilibrium and bias. • Understand built-in potential, depletion width, and carrier distribution. • Analyze how carrier concentration varies with temperature.	**2 hours**
3.	I-V Characteristics of a Diode (Forward and Reverse Bias) • Analyze variation of I-V characteristics with temperature. • Study thermal generation and leakage in reverse bias.	**2 hours**
4.	Creating NMOS structure and simulation of I_D-V_{GS} and I_D-V_{DS} characteristics using TCAD tools, and extraction of the following parameters (i) Threshold voltage extraction (ii) Subthreshold slope extraction (iii) DIBL extraction (iv) Body coefficient extraction (v) Substrate and gate current extraction (vi) Breakdown voltage extraction (vii) Short channel device current	**4 hours**
5.	FinFET/Double-Gate MOSFET Design and Analysis • Simulate short-channel devices and compare to bulk MOSFET. • Study electrostatic control and channel leakage.	**2 hours**
6.	Design of a CMOS Inverter and Delay Analysis • Combine NMOS and PMOS models. • Perform transient simulation for inverter delay and power estimation.	**2 hours**
7.	Simulation of Thermal Oxidation of Silicon • Model dry and wet oxidation processes. • Compare oxide thickness and growth rate using Deal-Grove model.	**4 hours**
8.	Ion Implantation and Dopant Diffusion • Simulate implantation of Boron and Phosphorus. • Analyze depth profiles before and after annealing.	**2 hours**
9.	Silicon wafer dicing, cleaning, and Oxidation of silicon wafer	**2 hours**
10.	Thermal Evaporation of metal onto a Silicon substrate	**2 hours**
11.	Optical microscopy characterization of the deposited materials	**2 hours**
12.	I-V and C-V characteristics of fabricated MOSFET/MOS Capacitor	**4 hours**
	Total Laboratory Hours	**30 hours**

Mode Evaluation : Continuous Assessment and Final Assessment Test.			
Recommended by Board of Studies			
Approved by Academic Council	**No.**	**Date**	

Course Code	Course Title	L	T	P	C
MAVLDXXX	Digital IC Design	3	1	0	4
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

1. Apply the models for state-of-the-art VLSI components, fabrication steps and layout design techniques.
2. Focus on the systematic analysis and design of basic digital integrated circuits in CMOS technology.
3. Enhance problem solving and creative circuit design techniques.

Course Outcomes

1. Design of the CMOS inverter with optimized power, area and timing.
2. Design layout for various digital integrated circuits.
3. Interpret the performance of static and dynamic digital CMOS circuits.
4. Design of CMOS memory and arrays structures.
5. Interpret the interconnect modelling and Datapath structures.

Module:1	The CMOS Inverter	12 hours

Introduction to Digital IC Design, Issues in Digital IC Design, Quality Metrics of a Digital Design, Review of MOS Transistor Theory. Static CMOS Inverter- Static and Dynamic Behavioural Practices of CMOS Inverter – Noise Margin. Components of Energy and Power – Switching -Short-Circuit and Leakage Components. Technology scaling and its impact on the inverter metrics - Passive and Active Devices, PPA optimization of CMOS Inverter using EDA Tools.

Module:2	CMOS Fabrication and Layout	10 hours

CMOS Process Technology N-well, P-well process, SOI process, Stick diagram for Boolean functions, Optimization using Euler Theorem, Layout Design Rules, Layout of complex logic circuits.

Module:3	CMOS Combinational and Sequential Circuit Design	17 hours

Designing Fast CMOS Circuits -Logical Effort, Complementary CMOS -Ratioed Logic (Pseudo NMOS, DCVSL) - Pass Transistor Logic - Transmission gate logic - Dynamic Logic Design Considerations - Speed and Power Dissipation of Dynamic logic -Signal integrity issues -Domino Logic. Introduction - Static Latches and Registers - Dynamic Latches and Registers - Pulse Based Registers - Sense Amplifier based registers. Setup and Hold time calculation. PPA optimization of CMOS Combinational and Sequential Circuit using EDA Tools.

Module:4	Designing Memory & Array structures	10 hours

SRAM and DRAM Memory Core - memory peripheral circuitry – Memory Cell Stability-Memory reliability and yield - Power dissipation in memories. Memory Design issues and Challenges, Various Memory bit cell and design metrics. Design analysis of Memory structures using EDA Tools.

Module:5	Interconnects and Datapath Structures	9 hours

Resistive, Capacitive and Inductive Parasitics - Computation of R, L and C for given interconnects - Capacitance and Reliability -Resistance and Reliability - The Full Adder: Circuit Design Considerations - Barrel Shifter - Power and Speed Trade-off's in Datapath Structures.

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	60 hours

Text Books				
1	Jan M. Rabaey, AnanthaChadrakasan and BorivojeNikolic, Digital Integrated Circuits: A Design Perspective, 2016, Second Edition, PHI.			
2	Neil.H, E.Weste, David Harris and Ayan Banerjee, CMOS VLSI Design: A Circuit and Systems Perspective, 2015, Fourth Edition, Pearson Education.			
Reference Books				
1.	Sung-Mo Kang, Yusuf Leblebici, CMOS Digital Integrated Circuits - Analysis and Design, 2014, Fourth Edition, McGraw-Hill.			
2.	Sorab K Gandhi, VLSI Fabrication Principles: Si and GaAs, 2010, Second Edition, John Wiley and Sons.			
3.	Ivan Sutherland, R. Sproull and D. Harris, "Logical Effort: Designing Fast CMOS Circuits", 1999, Publisher: Morgan Kaufmann.			
4.	Jawar Singh, Saraju P. Mohanty, Dhiraj K. Pradhan, "Robust SRAM Designs and Analysis", 2013, Springer-Verlag New York.			
Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT				
Recommended by Board of Studies		DD-MM-YYYY		
Approved by Academic Council		**No.**	**Date**	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	Digital System Design with FPGA	3	0	2	4
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

1. Introduce the fundamentals of Verilog HDL and different levels of modeling.
2. Equip students with modeling of combinational and sequential circuit implementation.
3. Prepare students to model subsystem and system implementation on FPGA.

Course Outcomes

1. Utilize the Verilog HDL constructs to model the combinational and sequential logic circuits.
2. Implement the data path and controller design for customized specification.
3. Design memory and simple processor using Verilog HDL.
4. Interpret various FPGA architectures
5. Utilize simulation and synthesis tools to design, verify, and implement digital circuits on FPGA platforms.

Module:1	Verilog HDL Modeling	13 hours

Gate Level Modeling - Data Flow Modeling - Behavioral level Modeling - Tasks & Functions – Test Bench – Delay - System Tasks & Compiler Directives - Synthesizable Coding Style.

Module:2	Modeling of Combinational And Sequential Logic Design	10 hours

Design and Modeling of Combinational Circuits using Verilog HDL - Ripple carry Adder, Carry look ahead adder , Unsigned binary Multipliers. FSM design modeling using Verilog HDL - Sequence detector , Serial adder, Vending machine. Synthesizable Coding Style for Sequential Circuits and FSM, Datapath and Controller, Binary Counter, Bus Protocols.

Module:3	Modeling of Memory and Processor	8 hours

Single port and Dual port ROM and RAM, Memory Banks ,Synchronous and Asynchronous FIFO , Pipeline, Modeling of Simple Processor.

Module:4	FPGA Architecture	6 hours

Types of Programmable Logic Devices - PLA, PAL, CPLD, FPGA Generic Architecture - Programming Technologies- I/O Banks - Programmable Logic Blocks, Realization of combinational and sequential functions using CLB , Xilinx/ Intel / Actel FPGA Architecture - Case Study.

Module:5	FPGA Design Implementation	6 hours

Interfacing ADC / DAC using SPI Protocol, Interfacing External device using UART, Partial Reconfiguration.

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours

Text Books	
1	Lin, Ming-Bo, Digital system designs and practices: using Verilog HDL and FPGAs, Second Edition, Wiley Publishing, 2008.
2	Michael D Ciletti, Advanced Digital Design with the Verilog HDL, Second Edition, 2017, Pearson Education.
Reference Books	
1.	Shirshendu Roy , Advanced Digital System Design: A Practical Guide to Verilog Based FPGA and ASIC Implementation ,2024, Springer
2.	Wayne wolf, FPGA Based System Design, 2011, Prentices Hall Modern Semiconductor Design Series.

Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT

List of Experiments (Indicative)	
Schematic based combinational circuit design & implementation –	**2 hours**
Block Level / IP based combinational / sequential circuit design & Implementation	**2 hours**
Design of Combinational Circuit using Verilog HDL and Verification using testbench -Modelsim	**2 hours**
Complex Combinational Circuit Design & Implementation using seven segment display in FPGA board	**2 hours**
Complex Sequential Circuit Design & Implementation using seven segment display in FPGA board	**2 hours**
Sequential Circuit Design & Implementation / Timing Analysis /Power Analysis	**2 hours**
FSM based Design & Implementation	**2 hours**
Memory Modeling & Implementation	**2 hours**
Datapath and Controller - Design and Implementation	**2 hours**
Simple Processor - Design and Implementation	**2 hours**
Total Laboratory Hours	**30 hours**

Mode Evaluation: Mini Project , Continuous Assessment and Final Assessment Test**.**

Recommended by Board of Studies	DD-MM-YYYY		
Approved by Academic Council	**No.**	**Date**	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	Analog IC Design	3	0	2	4
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

1. Develop a strong foundation in analog circuit design using MOSFETs
2. Analyze the frequency response of amplifiers, feedback amplifiers, noise analysis and stability.
3. Explore AI/ML applications in analog IC design, focusing on automated performance optimization and industry-driven methodologies

Course Outcomes

1. Analyze MOS transistor models and their impact on frequency response and noise characteristics to design efficient single-stage and differential amplifiers.
2. Design CMOS Operational Amplifiers by employing AI/ML-based optimization methods for performance enhancement.
3. Apply frequency compensation and feedback techniques to enhance stability and minimize distortion in amplifier design.
4. Analyze Bandgap References and Phase-Locked Loop (PLL) circuits.
5. Design single-stage and differential amplifiers, applying industry-standard EDA tools to optimize circuit performance and meet design specifications

Module:1	Fundamentals of Analog IC Design	9 hours

Overview of Analog blocks in SoC Design, MOS Device Models & Circuit Basics, Current Sources & Current Mirrors, Single-Stage Amplifiers-Common Source, Common Gate, Source Follower, Cascode, Differential Amplifiers-Single-Ended vs. Differential Operation, Basic Differential Pair.

Module:2	Frequency Response, Noise & Feedback	9 hours

Miller Effect & Frequency Response Analysis in Single Stage and Differential Amplifiers, Noise in Amplifiers: CS, CG, Source Follower, Cascode, Differential Pair, Noise Bandwidth Considerations, Feedback Amplifiers: Negative Feedback, Distortion Reduction, Feedback Configurations: Voltage-Voltage, Current-Voltage, Current-Current, Voltage-Current.

Module:3	CMOS Operational Amplifiers Design	9 hours

Need for Single & Multistage Amplifiers, Single Stage Amplifiers-Telescopic, Folded, Gain Boosting, Two-Stage Op-Amps, Frequency Response of Two Stage OpAmp, Performance Parameters of Two Stage OpAmps, Common Mode Feedback-CMRR, PSRR, AI/ML-based Op-Amp performance optimization- Automated Tuning using ML algorithms.

Module:4	Stability & Frequency Compensation	6 hours

Concepts of Stability: Gain Margin, Phase Margin, Frequency Compensation Techniques- Dominant Pole, Miller Compensation, Compensation of Miller RHP Zero, Nested Miller Compensation, Stability Criterion-Nyquist and Bode Plot, Practical Circuit Design Consideration.

Module:5	Bandgap References and PLL	10 hours

Bandgap Reference Circuits-Supply-Independent Biasing, PTAT Current Generation, PLL Concepts-Phase Detector, Basic PLL & Charge Pump PLL, Non-Ideal Effects in PLL-PFD and Charge Pump Non-Idealities, Clock Jitter.

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours

Text Book(s)			
1.	Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2017, 2nd Edition, McGraw-Hill		
2.	Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2016, 2nd Edition, Oxford University Press.		
Reference Books			
1.	Behzad Razavi, Design of CMOS Phase-Locked Loops, 2020, Cambridge University Press.		
2.	R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, 2010, 3rd Edition, IEEE Press, Wiley Publications.		
3.	Ren, H., and Hu, J., Machine Learning Applications in Electronic Design Automation. 2022, 1st Edition, Springer.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
List of Experiments (Indicative)			
Simulation of MOSFET IV Characteristics & Second-Order Effects, g_m/I_D plots.			**4 hours**
Design of simple current mirror and cascode current mirror.			**2 hours**
Design of Single Stage Amplifiers- Common Source, Common Gate and Common Drain.			**4 hours**
Analysis and Design of Differential Amplifier with Active load and Current Source Load.			**4 hours**
Layout of differential amplifier and post-layout simulation.			**4 hours**
Design of Cascode Amplifiers.			**4 hours**
Analysis and Design of Two-Stage op-amp with Frequency Compensation.			**6 hours**
Noise analysis of single stage amplifier and Differential Amplifiers.			**2 hours**
Total Laboratory Hours			**30 hours**
Mode of Evaluation: Digital Assignment and Final Assessment Test			
Recommended by Board of Studies		**DD-MM-YYYY**	
Approved by Academic Council	No. xx	Date	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	ASIC Design	3	0	2	4
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

1. Understand the fundamental of ASIC design flow with respect to different cost functions.
2. Recognize the importance of formal verification and static timing analysis in ASIC design.
3. Comprehend the guidelines at each abstraction level in physical design and Verification

Course Outcomes

1. Demonstrate ASIC design flow and the issues related to synthesis including technology choice, design environment and constraints.
2. Apply formal verification techniques such as equivalence checking and property checking in the context of ASIC development.
3. Interpret the timing behavior of digital circuits using Static Timing Analysis techniques.
4. Apply design rules, methods, and timing concepts to create efficient physical designs and resolve issues like congestion, IR drop, and electromigration.
5. Utilize industry-standard EDA tools to implement, test and verify physical design stages.

Module:1	RTL Synthesis	9 hours

ASIC Design methodology: Custom IC Design - Cell-based Design Methodology - Array based implementation approaches - Traditional and Physical Compiler based ASIC Flow. RTL synthesis: RTL Synthesis Flow - Synthesis Design Environment & Constraints – Architecture of Logic Synthesizer - Technology Library Basics– Components of Technology Library –Synthesis Optimization- Technology independent and Technology dependent synthesis- Data path Synthesis – Low Power Synthesis.

Module:2	Formal Verification	6 hours

Combinational Equivalence Checking- Constrained EC - Cut Point-Based EC - Sequential Equivalence Checking - Register Correspondence - Model Checking - Property Checking.

Module:3	Static Timing Analysis	12 hours

Timing Parameter Definition – Setup Timing Check- Hold Timing Check - Setup and Hold Violation Fixing - Multicycle Paths- Half-Cycle Paths- False Paths - Clock skew optimization – On-Chip Variations- AOCV-POCV-Time Borrowing- Setup and Hold Violation Fixing. Origins of Clock Skew/Jitter and impact on Performance. Clock Domain Crossing – Synchronizers.

Module:4	Physical Design	8 hours

Detailed steps in Physical Design Flow - Guidelines for Floor plan, Placement, CTS and routing – ECO flow – Signal Integrity Issues – Crosstalk.

Module:5	Physical Design Verification	8 hours

Timing Sign-off, Physical Verification – Signoff DRC and LVS, ERC, IR Drop Analysis, Antenna Check, Electro-Migration Analysis and ESD Analysis.

Module:6	Contemporary Issues	2 hours
	Total hours:	45 hours

Text Book(s)

1.	Vaibbhav Taraate, ASIC Design and Synthesis, 2021, First Edition, Springer.
2.	Sneh Saurabh, Introduction to VLSI Design Flow, 2023, Cambridge University Press.

Reference Books

1.	Khosrow Golshan, PHYSICAL DESIGN ESSENTIALS: An ASIC Design Implementation Perspective, 2010, First Edition, Springer.
2.	Andrew B. Kahng, VLSI Physical Design: From Graph Partitioning to Timing Closure, Springer International Publishing, 2022
3.	J. Bhasker and Rakesh Chadha, Static Timing Analysis for Nanometer Designs, 2010, First Edition, Springer, USA.

Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT

List of Experiments (Indicative)

Design of Digital Architecture for the given specification - Design of SPI / Design of a simple CPU	6 hours
Logical Synthesis of Digital Architecture	4 hours
Netlist Optimization, GLS and Formal Verification	4 hours
Physical design of Digital Architecture	10 hours
Physical verification of Digital Architecture	2 hours
Case study: Implementation of Digital Architecture using UPF.	4 hours
Total Laboratory Hours	**30 hours**

Mode of Evaluation: Digital Assignment and Final Assessment Test

Recommended by Board of Studies	DD-MM-YYYY		
Approved by Academic Council	No. xx	Date	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	VLSI Testing and Testability	3	0	2	4
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

1. Impart knowledge on the importance of VLSI testing and fault modeling across different levels of design abstraction.
2. Prepare the learners to design more robust testable VLSI circuits with various Design for Testability (DFT) strategies.
3. Develop proficiency in test generation, fault simulation, and memory test strategies, including diagnostic and self-repair mechanisms to ensure reliable VLSI system design.

Course Outcomes

1. Explore various fault models and testing strategies applicable at different abstraction levels in the VLSI design flow.
2. Apply Design for Testability (DFT) techniques to enhance the testability of digital circuits, I/Os and interconnects.
3. Apply the fault simulation and test generation algorithms to test both combinational and sequential circuits.
4. Apply memory test algorithms and MBIST to test memory, and diagnose and repair the defects.
5. Implement modifications to a given digital circuit, system and memory, and make it testable using the various testability methods with EDA tools.

Module:1	Testing and Fault Modeling	7 hours

Importance of testing - Testing during the VLSI lifecycle - Fault models: Stuck-at faults, Transistor faults, open and short faults, Delay faults and crosstalk, Pattern sensitivity and coupling faults, Analog fault models – Fault equivalence and fault collapsing - Levels of abstraction in VLSI testing - Review of VLSI test technology - SCOAP testability analysis

Module:2	Design for Testability	10 hours

Design for Testability: Ad-hoc approach, Structured approach - Scan cell designs, Scan architectures, Scan Design Rules, Scan Design Flow - Special-Purpose Scan Designs - RTL Design for Testability.
Logic BIST: BIST Design Rules - Test Pattern Generation: LFSR – Output Response analysis: Signature Analysis- Logic BIST architectures for circuits with scan chain – BIST architectures using register reconfiguration.

Module:3	Fault Simulation and Test Generation	7 Hours

Fault Simulation: Parallel, Concurrent and Deductive - Alternative to Fault Simulation.
Test Generation: Combinational ATPG: D-Algorithm - Sequential ATPG: Time frame expansion - Untestable Fault Identification - ATPG for non-stuck-at faults.

Module:4	Memory Testing and Repair	12 hours

RAM Functional Fault Models and Test Algorithms - RAM Fault Simulation and Test Generation - Memory Built-In Self-Test. BIST with Diagnostic Support - RAM Defect Diagnosis and Failure Analysis - Built-In Self-Repair.

Module:5	Test Data Compression and Board Level Testing	7 hours

Test Compression: Linear decompression-based schemes, Broadcast scan-based schemes - Test response compaction: Space compaction, Time compaction, Mixed time and space compaction.
Board level Testing: Digital boundary scan (IEEE Std.1149.1) – Embedded Core Test Standard (IEEEStd.1500)

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours

Text Books

1	Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, 2013, VLSI Test Principles and Architectures, The Morgan Kaufmann.
2	M. Bushnell, Vishwani Agrawal - Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, 2006, Springer.
Reference Books	
1.	Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "System-on-chip Test Architectures: Nanometer Design for Testability", 2008, Morgan Kaufmann Publishers.
2.	Sebastian Huhn, Rolf Drechsler, "Design for Testability, Debug and Reliability Next Generation Measures Using Formal Techniques" 2021, 1st ed. Springer.
Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT	
List of Experiments (Indicative)	
Stuck-at-fault and IDDQ Testing by Simulation	**4 hours**
DFT Synthesis of complex Sequential circuits: fixing of DFT rule violation, Scan insertion	**6 Hours**
ATPG, Fault simulation and Analysis (Stuck-at-faults, Transition faults, at-speed test with OCC– LoC and LoS)	**4 hours**
Testing of Digital circuits using Logic BIST	**4 hours**
Testing of RAM using MBIST	**4 hours**
Testing of SoC containing Logic Core, Custom IP, Boundary scan , Memory, Test compression architecture) with IJTAG, MBIST, Test compression	**8 hours**
Total Laboratory Hours	**30 hours**
Mode of Evaluation : Continuous Assessment and Final Assessment Test.	

Recommended by Board of Studies	DD-MM-YYYY		
Approved by Academic Council	**No.**	**Date**	DD-MM-YYYY

Course Code	Course title	L	T	P	C
MAVLDXXX	Low Power IC Design	3	0	0	3
Pre-requisite		Syllabus version			
MAVLDXXX	Digital IC Design	1.0			

Course Objectives:

1. Understand the Need for Low Power Design and learn sources of power dissipation.
2. Design various circuits with optimal power consumption by addressing challenges at various design levels
3. Design a system with multiple supply and threshold voltages applicable for various applications

Course Outcomes:

1. Utilize probabilistic methods to estimate power consumption of VLSI circuits.
2. Employ power optimization techniques at system , RTL and circuitlevel.
3. Apply various leakage power reduction techniques to minimize the power in nano scale VLSI circuits.
4. Implement the power intent in low power automation.

Module:1	Power Estimation	10 hours

Motivation- Context and Objectives-Sources of Power dissipation deep submicron circuits - Revision Effects of scaling on power consumption- Low power design flow- Normalized Figure of Merit – PDP& EDP- Overview of power optimization at various levels. Need for Power - Estimation – Calculation of Steady state probability, Transition probability, Conditional probability, Transition probability of correlated inputs, Transition density; Estimation of Switching activity, Estimation of glitching power.

Module:2	System Level Optimization	9 hours

Software level power optimization. Pipelining, Parallel Processing and retiming approaches for power minimization,Clock Gating, Dynamic Voltage Scaling (DVS), Dynamic Voltage and Frequency Scaling (DVFS), Multi VDD Designs - Choice and Placement of Level shifters , Low power clock design.

Module:3	RTL and Circuit Level Optimization	11 hours

Low power memory design - SRAM architectures. Pre-computation, Data gating, Bus Encoding techniques, Deglitching for low power, Synthesis of FSM for low power. Transistor variable re-ordering for power reduction, , Optimal drivers of high-speed low power ICs, Low power library cell design (GDI). Circuit techniques for reducing power consumption in Adders, Multipliers.

Module:4	Leakage Power Reduction	8 hours

Leakage power reduction techniques-stacking techniques, sleepy keeper technique, super cut off CMOS, VTCMOS, MTCMOS, DTCMOS- energy constrained and delay constrained. Sleep Transistor Design- switch efficiency, area efficiency, IR drop, normal Vs reverse body bias. Inrush current and current latency. Power gating – coarse grain and fine grain. Isolation, retention, power down and wake up methods. Leakage power reduction in FinFET based circuits.

Module:5	Automation for Low Power	5 hours

Low power design techniques automation levels, Power-Aware design flow, Unified power format (UPF): Necessity, UPF tutorial, Low power design example using UPF, Design flow modification with UPF.

Module:6	Contemporary issues	2 hours
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	Kaushik Roy, Sharat Prasad, Low Power CMOS VLSI circuit design, 2010, Second Edition, John Wiley and Sons Inc.
2.	Ajit Pal , Low Power VLSI circuits and Systems, 2014, First Edition, Springer, India,
Reference Books	
1.	Gary K.Yeap, Practical Low Power Digital VLSI Design, 2010, First Edition, Springer, US.
2.	Jan M.Rabaey, Massoud Pedram, Low power Design methodologies, 2014, First Edition, Springer, US.
3.	Soudris, Dimitrios, Christrian Pignet, Goutis, Costas, Designing CMOS circuits for low power, 2011, First Edition, Springer, US.
4	Abdellatif Bellaouar, Mohamed Elmasry,Low-Power Digital VLSI Design, Circuits and systems,2019,Second Edition, Springer /MBS.
5	S. Ramamurthy,Low Power Digital VLSI Design Circuits and Systems , First Edition, 2014, Medtec.
6	Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, Kaijian Shi, Low power methodology manual: for system-on-chip design, 2007, Springer Science & Business Media.
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.	

Recommended by Board of Studies		DD-MM-YYYY	
Approved by Academic Council	No. xx	Date	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	VLSI Verification Methodologies	3	0	2	4
Pre-requisite		Syllabus Version			
MAVLDXXX	Digital System Design with FPGA	1.0			

Course Objectives

1. To introduce various verification techniques.
2. To write Test bench using System Verilog.
3. To develop UVM test environment

Course Outcomes

1. Illustrate verification methods and System Verilog language constructs.
2. Implement verification environment using System Verilog
3. Examine coverage metrics and assertions
4. Employ industry-standard framework for verification
5. Apply various verification techniques to verify complex VLSI designs

Module:1	Introduction to Verification	5 hours

Introduction to Verification – DUT - Functional Verification – Testplan - Self-checking Test bench (Linear & Task-based) - Regression - RTL Formal Verification – Coverage

Module:2	System Verilog Language Basics	10 hours

Introduction to System Verilog — Literal values-data Types — Arrays — Array methods — Creating new types with type def — user defined structures — Enumerated types — attributes - operators — expressions - Procedural statements and control flow - Processes in System Verilog — Task and functions — Routine arguments — Returning from a routine - OOP Terminology - Creating Object - Object Deallocation - Copying Objects - Static variables - Global variables – Inheritance – Polymorphism

Module:3	System Verilog Verification Environment	10 hours

Program, Interface, Stimulus timing, Module interactions, Connecting together, Development of self-checking test environment — Transaction/Data, Generator, Driver, Monitor, Scoreboard, Randomization in system Verilog – Constraints – Controlling multiple constraint blocks – In-line constraints - Verification of RAM.

Module:4	Verification Techniques in System Verilog	8 hours

Coverage Types – Anatomy of covergroup – Triggering a covergroup, Data Sampling, – Cross Coverage – Coverage options, Evolution of System Verilog Assertions– SVA Assertion Methodology – Immediate Assertions – Concurrent Assertions - Operators – SVA Applications – Clock domain crossing Verification – Low Power Verification

Module:5	Universal Verification Methodology	10 hours

Introduction to UVM - Verification components - Transaction level modeling - Developing reusable verification components - Using Verification components — Developing reusable verification environment — Register classes — Bus Protocol Verification (AHB/APB).

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours

Text Books			
1	Ashok B. Mehta, Introduction to System Verilog, 2021, Springer, New York.		
2	Srivatsa Vasudevan, Practical UVM Step by Step with IEEE 1800.2, 2020, Second edition, R R Bowker, CA, USA.		
Reference Books			
1.	Ashok B. Mehta, ASIC/SoC Functional Design Verification – A Comprehensive guide to Technologies and Methodologies, 2017, First Edition, Springer.		
2.	Christian B Spear, System Verilog for Verification: A guide to learning the Testbench language features, 2012, Third Edition, Springer publications.		
3.	Vanessa R. Copper, "Getting started with UVM: A Beginner's Guide", 2013, First Edition, Verilab Publishing		
Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT			
List of Experiments (Indicative)			
1. Linear & Task – based self-checking test environment			**6 hours**
2. System Verilog Arrays			**2 hours**
3. Inter process communication (Mailbox)			**4 hours**
4. Developing self-checking test environment			**6 hours**
5. Functional Coverage			**2 hours**
6. System Verilog Assertions			**4 hours**
7. Developing UVM based self-checking test environment			**6 hours**
Total Laboratory Hours			**30 hours**
Mode of Evaluation : Continuous Assessment and Final Assessment Test.			
Recommended by Board of Studies			DD-MM-YYYY
Approved by Academic Council	**No.**	**Date**	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	MIXED SIGNAL IC DESIGN	3	0	0	3
Pre-requisite		Syllabus Version			
MAVLDXXX	Analog IC Design	1.0			

Course Objectives

1. Develop an ability to understand the Sampling and Switched Capacitor Circuits
2. Comprehend the fundamentals and architectures of ADCs and DACs
3. Familiarize with oversampling converter

Course Outcomes

1. Interpret the theory of Sampling and Sampling Circuits
2. Design CMOS based Switched Capacitor Circuits
3. Design the architectures of ADCs and DACs
4. Analyze the oversampling converter architecture

Module:1	Sampling and Sampling Circuits	9 hours

Introduction – sampling - Spectral properties of sampled signals - Oversampling – Anti-alias filter design. Time Interleaved Sampling - Ping-Pong Sampling System - Analysis of offset and gain errors in Time Interleaved Sample and Hold.

Sampling circuits- Distortion due to switch - Charge injection - Thermal noise in sample and holds - Bottom plate sampling - Gate bootstrapped switch - Nakagome charge pump. Characterizing Sample and hold - Choice of input frequency.

Module:2	Switched Capacitor Circuits	6 hours

Switched Capacitor (SC) circuits– Parasitic Insensitive Switched Capacitor amplifiers - Non idealities in SC Amplifiers – Finite gain - DC offset - Gain Bandwidth Product. Fully differential SC circuits - DC negative feedback in SC circuits.

Module:3	Fundamentals of A/D and D/A Converters	6 hours

Data converter fundamentals: Offset and gain Error - Linearity errors - Dynamic Characteristics – SQNR - Quantization noise spectrum.

Module:4	A/D and D/A Converters Architectures	14 hours

Flash ADC - Regenerative latch - Preamp offset correction - Preamp Design - necessity of up-front sample and hold for good dynamic performance. Folding ADC - Multiple-Bit Pipeline ADCs and SAR ADC.

DAC spectra and pulse shapes - NRZ vs RZ DACs. DAC Architectures: Binary weighted - Thermometer DAC - Current steering DAC - Current cell design in current steering DAC - Charge Scaling DAC - Pipeline DAC.

Module:5	Oversampling Converter	8 hours

Benefits of Oversampling -Oversampling with Noise Shaping - Signal and Noise Transfer Functions - First and Second Order Delta-Sigma Converters. Introduction to Continuous-time Delta Sigma Modulators - time-scaling - inherent antialiasing property - Excess Loop Delay - Influence of Op-amp non idealities - Effect of Op-amp non idealities - finite gain bandwidth - Effect of ADC and DAC non idealities - Effect of Clock jitter.

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours

Text Books				
1	David Johns and Ken Martin, Analog Integrated Circuit Design, 2012, Second Edition John Wiley & Sons Inc.			
2	Frank Ohnhauser, Analog-Digital Converters for Industrial Applications Including an Introduction to Digital-Analog Converters, 2015, First Edition, Springer Publishers.			
Reference Books				
1.	R Jacob Baker, CMOS Mixed-Signal Circuit Design, 2008, Second Edition, Wiley & IEEE			
2.	Ahmed M.A.Ali, High Speed Data Converters, 2016, First Edition, IET Materials, Circuits & Devices.			
Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT				
Recommended by Board of Studies		DD-MM-YYYY		
Approved by Academic Council		**No.**	**Date**	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	CAD for VLSI	3	1	0	4
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

1. Understand graph fundamentals, their relevance in VLSI design automation, and the basics of computational complexity and problem classes.
2. Explain and demonstrate partitioning, floor planning, area routing, clock routing, and pin assignment in the physical design flow using relevant algorithms and examples.
3. Introduce machine learning concepts and their applications in physical design.

Course Outcomes

1. Analyze graphs for given problems and the computational complexity of physical design algorithms.
2. Illustrate effective partitions for any given design.
3. Investigate optimized floor plans and placements.
4. Implement complex netlist and clock net routing meeting desired constraints.
5. Apply machine learning concepts in computer-aided design for VLSI.

Module:1	Graph theory and Computational complexity of algorithms	5 hours

Y Chart- Physical design top-down flow- Review of graph theory: complete graph, connected graph, sub graph, isomorphism, bi partite graph tree. Big-O notation- Class P, NP, NP-hard, NP-complete.

Module:2	Partitioning	12 hours

Problem formulation, Kernighan-Lin (KL) Algorithm, Extensions of the KL Algorithm, Fiduccia-Mattheyses (FM) algorithm, Simulated annealing based Partitioning, A Framework for Multilevel Partitioning.

Module:3	Floor planning and Placement	15 hours

Problem formulation, Stock Meyer algorithm- Wong-Liu algorithm (Normalized polish expression), Sequence pair technique. Pin Assignment: Concentric circle mapping, Topological pin assignment- Power and ground routing. Placement: Wire length estimation models for placement, Min-Cut Placement, Quadratic placement. Machine Learning for Datapath Placement

Module:4	Routing	14 hours

Routing: Grid routing- Maze routing- Line Probe algorithms, Weighted Steiner tree approach. Global routing: Rectilinear routing (spanning tree, Steiner tree)-Dijkstra's algorithm, Integer Linear Programming (ILP) based global routing. Detailed routing: Problem formulation- Two-layer channel routing: Left Edge algorithm, Dogleg router- Net Merge channel router - Switch box routing. Machine Learning for Routability-Driven Placement.

Module:5	Specialized Routing	12 hours

Clocking tree topologies: H-tree, Xtree - Method of Means and Medians (MMM) - Recursive Geometric Matching (RGM) - Elmore delay model to calculate skew- Buffer insertion in clock trees- Exact Zero skew and bounded-skew clock routing algorithm. Clock mesh topologies: uniform and non-uniform mesh. Machine Learning for Clock Optimization.

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	**60 hours**

Text Books				
1	Andrew B. Kahng, Jens Lienig, Igor L. Markov, JinHu, VLSI Physical Design: From Graph Partitioning to Timing Closure, 2022, Second edition, Springer International Publishing.			
2	Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, 2011, Springer, India.			
Reference Books				
1.	Rajesh K. Maurya , Ganesh M. Magar, Swati R. Maurya, Graph Theory & Applications, 2016, Technical Publications, India			
2.	Brian Christian and Tom Griffiths, Algorithms to Live By: The Computer Science of Human Decisions, 2017, First edition, William Collins, USA.			
3.	Elfadel, Ibrahim M., Duane S. Boning, and Xin Li, Machine learning in VLSI Computer-Aided Design, 2019, First edition, Springer, Switzerland.			
Mode of Evaluation: Quiz, Assignment, CAT and FAT				
Recommended by Board of Studies		DD-MM-YYYY		
Approved by Academic Council		**No.**	**Date**	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	System-on-Chip Design	3	1	0	4
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives:

1. Provide comprehensive knowledge of System-on-Chip architectures, design methodologies, and industry-standard tools.
2. Develop skills in interconnect design, timing/power optimization, and signal integrity analysis compliant with IEEE 1801 (UPF) and ISO 21434.
3. Implement FPGA-based SoC systems anddevelopment of customized IP blocks for applications.

Course Outcomes:

1. Demonstrate scalable SoC architectures.
2. Illustrate hardware-software co-design.
3. Interpret NoC topologies for latency and power efficiency.
4. Analyze FPGA-based SoC systems.
5. Apply customized IP blocks for SoC applications on FPGAs

Module:1	System-on-Chip (SoC) Fundamentals	9 hours
Evolution and trends in SoC design- Modern SoC architectures (e.g., RISC-V, ARM Cortex- A/M series) - Case studies: Apple M-series, NVIDIA SoCs.		
Module:2	**SystemC and HLS for SoC Design**	**13 hours**
Introduction to SystemC and Transaction-Level Modelling- Co-design, co-verification, simulation- Integration with Verilog/VHDL. HLS optimization techniques – Loop unrolling, pipelining, resource sharing, and their trade-offs.		
Module:3	**Network-on-Chip (NoC) Design**	**11 hours**
AMBA protocols (AHB, AXI) - Network-on-Chip: Routing, topologies, arbitration - Low-latency and fault-tolerant NoC design-UCIe, BOW, and optical NoCs.		
Module:4	**FPGA SoC Architecture and Design Flow**	**13 hours**
FPGA SoC Architecture - ARM Cortex A9 architecture – Nios V Softcore Processor – Configurable Hardware/ Software Design Flow.		
Module:5	**IP Core Based SoC Design**	**12 hours**
Clock Manager – Reset Controllers - Communication Protocol - Image edge detection algorithms Sobel, canny – Colour and Contrast Enhancement algorithm – Memory Controllers - Customized IP block Development Flow.		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**60 hours**

Text Book(s)

1. Michael J. Flynn, Wayne Luk,Computer System Design: System on chip, 2011, First Edition, Wiley-Blackwell.
2. Luca Benini, Giovanni De Micheli, Networks on Chips: Technology and Tools, Elsevier, 2021.

Reference Books

1. Martin S., System-on-Chip Design with Arm Cortex-M, 4th Ed., Arm Education, 2025.
2. Wayne Wolf, Modern VLSI Design: IP-Based Design, Pearson, *2020*.
3. Axel Jantsch, Modeling Embedded Systems and SoC using SystemC and TLM 2.0, Morgan Kaufmann, 2019.

Mode of Evaluation: Quiz, Assignment, CAT and FAT

Recommended by Board of Studies	DD-MM-YYYY		
Approved by Academic Council	**No.**	**Date**	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	Nano-scale Devices and Circuit Design	3	0	0	3
Pre-requisite		Syllabus Version			
MAVLDXXX	VLSI Devices and Technology	1.0			

Course Objectives

1. Understand the scaling concepts and physics of multi-gate devices.
2. Equip the students with the basic understanding of carbon nanowire FETs, TFETs and JLFETs
3. Acquire the knowledge of circuit design for multi-gate devices

Course Outcomes

1. Analyze short channel effects and multi-gate device technology along with channel, source/drain engineering.
2. Analyze the characteristics of nanowire transistors, CNT & graphene-based devices and SET devices.
3. Apply TFET and JLFET devices in digital circuits and memories.
4. Design digital circuits like SRAM and analog circuits like op amp, comparator using multi-gate devices.

Module:1	Introduction to Novel MOSFETs	7 hours

MOSFET scaling, short channel effects, channel engineering, source/drain engineering, high k dielectric, copper interconnects, strain engineering, SOI MOSFET, multi-gate transistors, single gate, double gate, triple gate, surround gate, quantum effects, volume inversion, mobility, threshold voltage, inter sub band scattering, multi-gate technology, mobility, gate stack.

Module:2	Physics of Multi-gate MOSFETs	9 hours

MOS Electrostatics, 1D, 2D MOS Electrostatics, MOSFET Current-Voltage Characteristics CMOS Technology, Ultimate limits, double gate MOS system, gate voltage effect, semiconductor thickness effect, asymmetry effect, oxide thickness effect, electron tunnel current, two-dimensional confinement, scattering, mobility

Module:3	Nanowire FETs and Transistors at the Molecular Scale	12 hours

Silicon nanowire MOSFETs, Evaluation of I-V characteristics, I-V characteristics for non-degenerate carrier statistics, I-V characteristics for degenerate carrier statistics, CNT, Band structure of CNT, CNT-FET, CNT-TUBFET, CNT-SET, CNT memories, CNT based switches, Logic Gates, CNT based RF devices, CNT based RTDs, Band structure of graphene, Electronic conduction in molecules, General model for ballistic nano transistors, MOSFETs with 0D, 1D, and 2D channels, Molecular transistors , Single electron charging, Single electron transistors

Module:4	Tunnel FETs and Junctionless FETs	9 hours

Basic TFET structure and working principle, Band diagram and device characteristics, ambipolar behavior of TFET, TFETS applications in digital circuits and memories, JLFET-Accumulation mode FET, Device structure and operation, Multi-gate JLFETs

Module:5	Circuit Design using Multi-gate Devices	6 hours

Digital circuits, impact of device performance on digital circuits, leakage performance trade off, multi-VT devices and circuits, SRAM design, analog circuit design, self-heating, band gap voltage reference, operational amplifier, comparator designs

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours

Text Books			
1	J P Colinge, FINFETs and other multi-gate transistors, Springer – Series on integrated circuits and systems, 2008		
2.	Jagadesh Kumar Mamida, Rajat Vishnoi, Pratyush Pandey, Tunnel Field-Effect Transistors Modelling and Simulation Wiley, 2017		
3.	Shubham Sahay Mamidala Jagadesh Kumar**,** Junctionless Field-Effect Transistors Design, Modeling, and Simulation, IEEE press Wiley 2019		
Reference Books			
1.	Mark Lundstrom Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, Springer, 2006		
2.	Balwinder Raj, Ashish Raman, Nanoscale Semiconductors Materials, Devices and Circuits, CRC press, 2023		
Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT			
Recommended by Board of Studies	DD-MM-YYYY		
Approved by Academic Council	**No.**	**Date**	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	RF IC Design	3	0	0	3
Pre-requisite		Syllabus Version			
MAVLDXXX	Analog IC Design	1.0			

Course Objectives

1. Understand the fundamentals of RF IC Design
2. Familiarize with the design of RF front-end circuits
3. Familiarize with the design of transceivers

Course Outcomes

1. Interpret the concepts of RF IC Design and importance of Impedance Matching.
2. Design of low noise, power amplifiers and mixers
3. Analyze of VCOs and frequency synthesizers.
4. Design the transceiver architectures.

Module:1	Introduction to RF IC Design and Metrics	5 hours

Basic concepts in RF Design: Nonlinearly - Time Variance – Inter symbol Interference - random processes - Noise. Definitions of sensitivity - dynamic range -conversion Gain and Distortion.

Module:2	High Frequency Model of MOS Transistors and Matching Networks	5 hours

MOSFET behavior at RF frequencies - Noise performance and limitation of devices - Impedance matching networks - transformers and baluns.

Module:3	RF Amplifiers and Mixers	13 hours

Low Noise Amplifiers: Common Source LNA - Common Gate LNA -Cascode LNA. Mixers: Design of Active and Passive Mixers. RF Power amplifiers - Class D, E and F

Module:4	VCOs and Frequency Synthesizers	10 hours

Basic topologies, Types of Oscillators- Cross coupled Oscillator, Three-point Oscillator, LC VCOs architecture, Tuning range with continuous and discrete, VCO phase noise, Quadrature Oscillators- basic concepts and topologies. Frequency Synthesizers: Types of Frequency divider - Integer-N and Fractional-N.

Module:5	Design of Transceiver	10 hours

System level Considerations, Receiver design, Transmitter design, Synthesizer design

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	**45 hours**

Text Books

1	B.Razavi, RF Microelectronics, 2013, Second Edition, Pearson Education Limited.
2	Hooman Darabi, Radio-Frequency Integrated Circuits and Systems, 2015, First Edition Cambridge University Press

Reference Books

1.	Gu, Qizheng, RF System Design of Transceivers for Wireless Communications, 2010, Springer.
2.	Bosco Leung, VLSI for Wireless Communication, 2011, Second Edition, Springer.

Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT

Recommended by Board of Studies	DD-MM-YYYY		
Approved by Academic Council	**No.**	**Date**	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	Advanced Computer Architecture	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

1. Introduce advanced concepts of computer architecture.
2. Acquire knowledge of various interconnect topologies for multiprocessor systems and different pipelining techniques.
3. Understanding different memory hierarchies for multiprocessor and multicomputer systems.

Course Outcomes

1. Apply different pipelining techniques to reduce computation time.
2. Illustrate interconnect architectures, hierarchical and shared memory architectures.
3. Interpret the Data level parallelism in Vector architecture, SIMD, GPU
4. Design multicore and multiprocessor architectures.

Module:1	Parallel computer models and Pipelining	10 hours

Classification of parallel computers - Data and resource Dependences - Hardware and software parallelism - Program partitioning and scheduling - Grain Size and latency - Program flow mechanisms - Control flow vs data flow - Data flow Architectures. Linear pipeline processor - nonlinear pipeline processor - Instruction pipeline Design - Mechanisms for instruction pipelining - Dynamic instruction scheduling - Branch Handling techniques - branch prediction Introduce heterogeneous computing models (CPU-GPU-FPGA combinations) – Introduction to multi-core system.

Module:2	System Interconnect Architectures and Memory Hierarchy Design	10 hours

Network properties and routing - Static interconnection Networks - Dynamic interconnection Networks - Multiprocessor system Interconnects - Hierarchical bus systems - Crossbar switch and multiport memory - Multistage and combining network. Cache basics - main memory organizations - design of memory hierarchies – Network on-chip interconnects (NoC)

Module:3	Data level Parallelism in Vector and GPU Architectures	10 hours

Vector Architecture- RISC-V Vector extension- Vector computation instructions, Registers and dynamic typing, loads and store, parallelism during vector execution, SIMD Instruction extension for multimedia-Graphics Processing Units- Detecting and enhancing loop-level parallelism, CUDA programming basics and GPU memory hierarchy Tensor Cores, AI-specific instructions - Architectural Simulation using gem5

Module:4	Shared Memory Architectures	7 hours

Symmetric shared memory architectures — distributed shared memory architectures — cache coherence protocols — scalable cache coherence — directory protocols — memory-based directory protocols — cache-based directory protocols -Cache coherence issues in multicore systems - NUMA architectures and optimization techniques

Module:5	Multiprocessor Architectures	6 hours

Computational models — An Argument for parallel Architectures — Scalability of Parallel Architectures — Benchmark Performances. Tiled Chip Multicore Processors(TCMP) - Future Trends and Optimizations.

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	**45 hours**

Text Books

1	Kai Hwang, NareshJotwani, Advanced Computer Architecture: Parallelism, Scalability, Programmability,Tata McGraw Hill Education Pvt. Ltd., India, Second Edition, 2011.

2	David Patterson, Andrew Waterman, The RISC-V Reader:An Open Architecture Atlas, 2017, First edition, Strawberry Canyon, USA.			
Reference Books				
1.	John L. Hennessy, David A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann, Fifth Edition, 2011.			
2.	DezsoSima, Terence Fountain, PeterrKarsuk Advanced computer Architectures – A Design Space Approach, Pearson, 2014.			
3.	J.P. Shen and M.H. Lipasti, Modern Processor Design, MC Graw Hill, Crowfordsville, 2005			
Mode of Evaluation: Quiz, Assignment, Design Project, CAT and FAT				
Recommended by Board of Studies		DD-MM-YYYY		
Approved by Academic Council		**No.**	**Date**	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	Neuromorphic Computing	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

1. Introduce the basics of neuromorphic computing, learning mechanisms and emerging memory technologies suitable for neuromorphic computing
2. Learn the design techniques of spiking neural networks with adaptive learning for different applications
3. Familarize with the design of fault-tolerant and reconfigurable neuromorphic systems

Course Outcomes:

1. Interpret how the neuromorphic systems differ from traditional computer architectures and computing paradigms
2. Illustrate the basic building blocks of spiking neural networks and synaptic weight update algorithms and design of spiking neural networks
3. Examine the emerging memory technologies suitable for neuromorphic computing
4. Design of hardware accelerators for machine learning.

Module:1	Introduction to Neuromorphic Computing Systems	7 hours

Concepts of artificial neural networks, basic principles of neuromorphic computing, difference from traditional computer architectures and computing paradigms, hardware models of spiking neurons, synaptic dynamics, synaptic plasticity mechanisms and learning, synthesizing real-time neuromorphic systems.

Module:2	Neuromorphic System Design	4 hours

Spiking neural networks, neural coding schemes, spiking neuron models, learning algorithms, synapses and inter-neuron communication, hardware accelerators for neuromorphic computing system.

Module:3	Learning Methods in Neuromorphic Systems	12 hours

Learning methods; conversion from ANN to SNN: converted SNNs, challenges of ANN conversion; supervised learning: tempotron, resumeme, spikprop algorithm, approximate derivation method; unsupervised learning: pair-based STDP learning rule, triplet STDP learning rule, reward-modulated STDP learning, other variants of STDP learning rule.

Module:4	Emerging Memory Devices for Neuromorphic Computing	10 hours

Introduction to memory; memory technology: SRAM, DRAM, STT-RAM, RRAM, resistive crossbar, phase change memory, other memory technologies; memory organization; in-memory computation for neuromorphic systems; dynamics of NVM synapse.

Module:5	Hardware Accelerators for Machine Learning	10 hours

Introduction to hardware accelerator systems for artificial intelligence and machine learning, vector architectures, FPGA, GPU and ASIC accelerators, in-memory computing accelerator design, neuromorphic accelerators, quantum neural network accelerators, energy-efficient deep learning inference on edge devices, hardware accelerator systems for embedded systems.

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours

Text Book(s)

1. Abderazek Ben Abdallah and Khanh N. Dang, "Neuromorphic Computing Principles and Organization", 2022, 1st Edition, Springer, Cham, Switzerland.
2. Khaled Salah Mohamed, "Neuromorphic Computing and Beyond- Parallel, Approximation, Near Memory, and

	Quantum", 2020, 1st Edition, Springer, Cham, Switzerland.			
Reference Books				
1.	Paul Miller, "An Introductory Course in Computational Neuroscience", 2018, Illustrated Edition, MIT Press, USA.			
2.	Wulfram Gerstner, Werner M. Kistler, Richard Naud and Liam Paninski, Neuronal Dynamics, 2014, Illustrated Edition, Cambridge University Press, USA.			
3.	Shiho Kim, Ganesh Chandra Deka, "Hardware Accelerator Systems for Artificial Intelligence and Machine Learning", 2021, 1st Edition, Elsevier Science, Netherlands.			
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test				
Recommended by Board of Studies		DD-MM-YYYY		
Approved by Academic Council		No. xx	Date	DD-MM-YYYY

Course Code	Course Title	L	T	P	C
MAVLDXXX	VLSI Digital Signal Processing	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

1. Familiarize with various representation methods of DSP algorithms, understand the significance of the iteration bound and calculate the same for a given single-rate and/or multi-rate DFG.
2. Understand and apply architectural transformation techniques, such as pipelining, parallel processing, retiming, unfolding and folding, to a given DFG.
3. Introduce algorithmic and numerical strength reduction methods for performance improvement.

Course Outcomes

1. Compute the iteration bound of a given single and/or multi-rate DFG.
2. Utilize pipelining, parallel processing and retiming techniques to transform the given DFG.
3. Apply unfolding and folding transformations to optimize given DFG.
4. Apply algorithmic and numerical strength reduction methods.

Module:1	Introduction to Digital Signal Processing Systems and Iteration Bound	9 hours

Typical DSP Algorithms - Representations of DSP Algorithms - Data-Flow Graph Representations. Loop Bound and Iteration Bound - Algorithms for Computing Iteration Bound: Longest Path Matrix and Multiple Cycle Mean algorithms - Iteration Bound of Multi-rate Data Flow Graphs.

Module:2	Pipelining, Parallel processing and Retiming	9 hours

Pipelining and Parallel Processing - Introduction to Retiming - Definitions and Properties - Solving Systems of Inequalities - The Bellman-Ford Algorithm - The Floyd Warshall Algorithm- Retiming Techniques.

Module:3	Unfolding and Folding	9 hours

Introduction, An Algorithm for Unfolding, Properties of Unfolding, Critical Path, Unfolding, and Retiming, Applications of Unfolding; Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures.

Module:4	Algorithmic Strength Reduction	8 hours

Introduction to Algorithmic Strength Reduction, Cook-Toom Algorithm, Iterated Convolution, Cyclic Convolution, Discrete Cosine Transform. Parallel FIR Filters. Parallel architectures for Rank-order filters

Module:5	Numerical Strength Reduction	8 hours

Introduction to Numerical Strength Reduction, Canonic Signed Digit Arithmetic, Distributed Arithmetic- Sub-expression Elimination, Multiple Constant Multiplication, Sub-expression Sharing in Digital Filters.

Module:6	Contemporary Issues	2 hours
	Total Lecture hours:	45 hours

Text Books	
1	Keshab. K.Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, 2014, Reprint, Wiley.
Reference Books	
1.	John G. Proakis, Dimitris K Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, 2015, Fourth Edition, Prentice Hall.
2.	Mohammed Ismail and Terri Fiez, Analog VLSI Signal and Information Processing, 2014, McGraw-Hill.
3.	S.Y. Kung, H.J. White House, T. Kailath, VLSI and Modern Signal Processing, 2010, PHI.
4.	S. K. Mitra, Digital Signal Processing – A Computer Based Approach, 2010, Fourth Edition, McGraw-Hill.
Mode of Evaluation: Quiz, Assignment, Design Project, Case Study, Seminar, CAT and FAT	

Recommended by Board of Studies		
Approved by Academic Council	**No.**	**Date**