



**Value-Added Course**  
**on**  
**VLSI Design using CADENCE Tools (VAC 1555)**  
**8<sup>TH</sup> February. 2026 to 5<sup>TH</sup> April 2026**

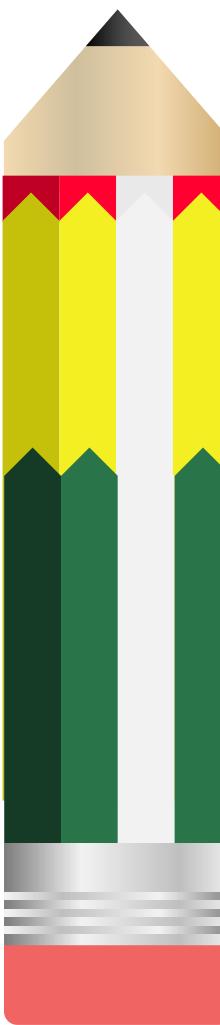
*Organized by*  
**Department of Micro & Nano Electronics (M & NE)**  
**School of Electronics Engineering (SENSE)**  
**VIT, Vellore - 632014**

| Advisory Committee   | Faculty Coordinators  |
|--|---|
| <p><b>Dr. Jasmin Pemeena Priyadarisini</b><br/><b>M, Dean, SENSE, VIT, Vellore -</b><br/><b>632014</b></p> <p><b>Dr. Sri Adibhatla Sridevi,</b><br/><b>HoD, Dept. of M &amp; NE, SENSE,</b><br/><b>VIT, Vellore - 632014</b></p> | <p><b>Dr. S. Ravi, Associate Professor, SENSE,</b><br/><b>VIT, Vellore - 632014</b></p> <p><b>Dr. Debashish Dash, Associate</b><br/><b>Professor, SENSE, VIT, Vellore - 632014</b></p> <p><b>Dr. Aarthy M, Assistant Professor,</b><br/><b>SENSE, VIT, Vellore - 632014</b></p> |

**Registration Details**

|                   | Important Dates   |
|-------------------|---|
| Registration Ends | <b>5<sup>th</sup> Feb. 2026</b>   |
| VAC Duration      | <b>8<sup>th</sup> Feb. 2026</b><br><b>21<sup>st</sup> - 22<sup>nd</sup> Feb. 2026</b><br><b>3<sup>rd</sup> - 5<sup>th</sup> Apr. 2026</b> |

**Payment (VIT QR Code)**



**Registration Fee: Rs. 500/-**  
**(including GST)**

## About VIT

VIT is committed to delivering world-class higher education through innovative practices, a diverse campus culture, and strong international collaborations. Supported by experienced faculty and motivated students, the university has earned prestigious global and national rankings, reflecting its excellence in teaching, research, sustainability, and academic impact.

## About the Course

The *Value-Added Course on VLSI Design* aims to introduce students to the most in-demand skills in the field of VLSI design. The course covers both the fundamental concepts and practical hands-on training required in VLSI development. Students will gain experience across the complete design flow. This comprehensive training enables students to efficiently manage design projects and build a strong foundation for a career as an **ASIC Design Engineer/VLSI Design Engineer**. Here, course will cover four different innovative VLSI tools.

- ❖ Cadence Virtuoso
- ❖ Cadence NCLaunch
- ❖ Cadence Genus
- ❖ Cadence Innovus

**21<sup>st</sup> February 2026**

- ❑ 10:30 – 12:30 PM: CMOS Layout **using Cadence Virtuoso**
- ❑ 2:30 – 4.30PM: Hands- on in CMOS Layout **using Cadence Virtuoso**

## About SENSE

SENSE at VIT was established for imparting state-of-the-art knowledge in Electronics and Communication Engineering and allied areas. B.Tech. Electronics and Communication Engineering is accredited by the Engineering Accreditation Commission of ABET. Students who are eligible are placed on campus and many of them are placed in core companies every year. The school has set up laboratories with excellent infrastructure in the areas of Electronics, Communication and VLSI, Embedded Systems and Sensor Systems.

## Topics to be Covered

**8<sup>th</sup> February 2026**

- ❑ 10:00 – 10:45 AM: VLSI Design Flow
- ❑ 11:00 – 1:00PM : Hands on Simulation of Basic CMOS Logic using **Cadence Virtuoso**
- ❑ 2:30 – 3.30PM: Performance Evaluation of CMOS Logic using Cadence Virtuoso

**22<sup>nd</sup> February 2026**

- ❑ 10:30 – 12:30 PM: CMOS Layout **using Cadence Virtuoso**
- ❑ 2:30 – 4.30PM: Hands- on in CMOS Layout **using Cadence Virtuoso**

**3<sup>rd</sup> April 2026**

- ❑ 10:30 – 12:30 PM: Introduction to Verilog HDL, Hands on simulation in **Cadence NCLaunch**
- ❑ 2:30 – 4.30PM: Hands- on synthesis on **Cadence Genus**

**4<sup>th</sup> April 2026**

- ❑ 10:30 – 12:30 PM: Gate Level Simulation, Static Timing Analysis (STA)
- ❑ 2:30 – 4.30PM: Physical Design Flow **using Cadence Innovus**

**5<sup>th</sup> April 2026**

- ❑ 10:30 – 12:30 PM: Mini Project (can be from analog or digital VLSI)
- ❑ 2:30 – 4.30PM: Valedictory & Feedback

**Venue: TT - 238**

**Total Duration 30 Hours**

**“E-Certificates will be provided for the registered participants”**