Value-Added Course
on
VLSI Design using CADENCE Tools (VAC 1555)
8TH February. 2026 to 5TH April 2026

Organized by

Department of Micro & Nano Electronics (M & NE)
School of Electronics Engineering (SENSE)
VIT, Vellore - 632014

Advisory Committee	Faculty Coordinators
Dr. Jasmin Pemeena Priyadarisini M, Dean, SENSE, VIT, Vellore – 632014 **Dr. Sri Adibhatla Sridevi, HoD, Dept. of M & NE, SENSE, VIT, Vellore - 632014**	**Dr. S. Ravi, Associate Professor, SENSE, VIT, Vellore – 632014** **Dr. Debashish Dash, Associate Professor, SENSE, VIT, Vellore – 632014** **Dr. Aarthy M, Assistant Professor, SENSE, VIT, Vellore – 632014**

Registration Details

	Important Dates
Registration Ends	**5th Feb. 2026**
VAC Duration	**8th Feb. 2026** **21st – 22nd Feb. 2026** **3rd - 5th Apr. 2026**

Registration Fee: Rs. 500/-
(including GST)

Payment (VIT QR Code)

About VIT

VIT is committed to delivering world-class higher education through innovative practices, a diverse campus culture, and strong international collaborations. Supported by experienced faculty and motivated students, the university has earned prestigious global and national rankings, reflecting its excellence in teaching, research, sustainability, and academic impact.

About SENSE

SENSE at VIT was established for imparting state-of-the-art knowledge in Electronics and Communication Engineering and allied areas. B.Tech. Electronics and Communication Engineering is accredited by the Engineering Accreditation Commission of ABET.
Students who are eligible are placed on campus and many of them are placed in core companies every year.The school has set up laboratories with excellent infrastructure in the areas of Electronics, Communication and VLSI, Embedded Systems and Sensor Systems.

About the Course

The *Value-Added Course on VLSI Design* aims to introduce students to the most in-demand skills in the field of VLSI design. The course covers both the fundamental concepts and practical hands-on training required in VLSI development. Students will gain experience across the complete design flow. This comprehensive training enables students to efficiently manage design projects and build a strong foundation for a career as an **ASIC Design Engineer/VLSI Design Engineer. Here, course will cover four different innovative VLSI tools.**

- **Cadence Virtuoso**
- **Cadence NCLaunch**
- **Cadence Genus**
- **Cadence Innovus**

Topics to be Covered

8th February 2026

- ❑ 10:00 – 10:45 AM: VLSI Design Flow
- ❑ 11:00 – 1:00PM : Hands on Simulation of Basic CMOS Logic using **Cadence Virtuoso**
- ❑ 2:30 – 3.30PM: Performance Evaluation of CMOS Logic using Cadence Virtuoso

21st February 2026

- ❑ 10:30 – 12:30 PM: CMOS Layout **using Cadence Virtuoso**
- ❑ 2:30 – 4.30PM: Hands- on in CMOS Layout using **Cadence Virtuoso**

22nd February 2026

- ❑ 10:30 – 12:30 PM: CMOS Layout **using Cadence Virtuoso**
- ❑ 2:30 – 4.30PM: Hands- on in CMOS Layout using **Cadence Virtuoso**

3rd April 2026

- ❑ 10:30 – 12:30 PM: Introduction to Verilog HDL, Hands on simulation in **Cadence NCLaunch**
- ❑ 2:30 – 4.30PM: Hands- on synthesis on **Cadence Genus**

4th April 2026

- ❑ 10:30 – 12:30 PM: Gate Level Simulation, Static Timing Analysis (STA)
- ❑ 2:30 – 4.30PM: Physical Design Flow using **Cadence Innovus**

5th April 2026

- ❑ 10:30 – 12:30 PM: Mini Project (can be from analog or digital VLSI)
- ❑ 2:30 – 4.30PM: Valedictory & Feedback

Venue: TT - 238

Total Duration 30 Hours

"E-Certificates will be provided for the registered participants "