VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING

B.Tech - Electronics Engineering (VLSI Design and Technology)

(B.Tech - BVD)

Curriculum

(*2024-2025 admitted students*)

VISION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

Transforming life through excellence in education and research.

MISSION STATEMENT OF VELLORE INSTITUTE OF TECHNOLOGY

World class Education: Excellence in education, grounded in ethics and critical thinking, for improvement of life.

Cutting edge Research: An innovation ecosystem to extend knowledge and solve critical problems.

Impactful People: Happy, accountable, caring and effective workforce and students.

Rewarding Co-creations: Active collaboration with national & international industries & universities for productivity and economic development.

Service to Society: Service to the region and world through knowledge and compassion.

VISION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

To be a leader by imparting in-depth knowledge in Electronics Engineering, nurturing engineers, technologists and researchers of highest competence, who would engage in sustainable development to cater the global needs of industry and society.

MISSION STATEMENT OF THE SCHOOL OF ELECTRONICS ENGINEERING

- Create and maintain an environment to excel in teaching, learning and applied research in the fields of electronics, communication engineering and allied disciplines which pioneer for sustainable growth.
- Equip our students with necessary knowledge and skills which enable them to be lifelong learners to solve practical problems and to improve the quality of human life.

B.Tech - Electronics Engineering (VLSI Design and Technology)

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

The **Program Educational Objectives (PEOs)** of B.Tech in Electronics Engineering (VLSI Design and Technology) program are as follows:

PEO1. **(Technical knowledge):** Graduates will have a sound knowledge on the fundamentals of mathematics, science, and electronics enabling them to analyse, design and test integrated circuits and systems.

PEO2. **(Professional growth / career):** Graduates will embrace their capability to expand horizons beyond engineering for academia, research, innovation and entrepreneurship.

PEO3. **(Soft skills):** Graduates will demonstrate their professional and ethical responsibilities with team spirit and engage in life-long learning.

B.Tech - Electronics Engineering (VLSI Design and Technology)

PROGRAMME SPECIFIC OUTCOMES (PSOs)

Upon on completion of the B.Tech in Electronics Engineering (VLSI Design and Technology), the graduates will be able to:

PSO1: Develop electronic circuits and systems with electronic materials to contribute for the global semiconductor ecosystem.

PSO2: Design, implement and test analog and digital integrated circuits and systems.

PSO3: Apply and develop the state of the art industry standard Electronic Design Automation for societal needs.

BECE203L	Circuit Theory	L	T	P	C
		3	1	0	4
Pre-requisite	**BEEE101L, BEEE101P**	**Syllabus version**			
		1.0			

Course Objectives

1. To prepare the students to analyse the given electrical network using phasors and graph theory.
2. To introduce the students with the basic knowledge of Laplace transform, Fourier Transform and Fourier series and to analyse the network using suitable technique.
3. To prepare the students to analyse the two-port networks, passive filters, and attenuators.

Course Outcome

1. Apply the knowledge of various circuit analysis techniques such as mesh analysis, nodal analysis, and network theorems to investigate the given network.
2. Analyse the resonance and transient response of the first order, second order circuits
3. Able to solve the networks using graphical approach.
4. Design and analyse two-port networks, passive filters and attenuators.
5. Able to analyse the given network by transforming from time domain to S domain.
6. Analyse the given network using Fourier series and transforming from time domain to frequency domain.

Module:1	**Sinusoidal Steady-State Analysis**	**10 hours**

Review of steady state sinusoidal analysis using phasors. Node voltage and Mesh current analysis, special cases. Network theorems: Superposition, Thevenin, Norton and maximum power transfer theorems.

Module:2	**Transient Response of first order, second order circuits and Resonance**	**10 hours**

Time response in inductance (L) and capacitance (C), steady state response of circuits with RLC components. Response (forced & natural) of first order circuits (RL & RC): series, parallel, source free, complex circuits with more than one resistance, power sources and switches. Response of second order circuit (RLC): series, parallel and complex circuits. Series and parallel resonance condition.

Module:3	**Network Graphs**	**6 hours**

Definition of terms. Matrices associated with graphs: incidence, reduced incidence, fundamental cut-set and fundamental tie-set.

Module:4	**Two-Port Networks**	**8 hours**

Significance and applications of one port and two port networks. Two port network analysis using Admittance (Y) parameters, Impedance (Z) parameters and Hybrid (h) parameters. Interconnection of Two port networks

Module:5	**Filters, Attenuators and equalizers**	**8 hours**

Concept of filtering. Filter types: Low-pass, High-pass, Band-pass and Band-stop and their characteristics. Design of attenuators: T, π, Lattice and Bridged-T types, Equalizers.

Module:6	**Circuit Analysis in the S domain**	**8 hours**

Introduction to Laplace transform (LT), poles, zeros and transfer functions. Analysis of first and second order circuits subjected to periodic and aperiodic excitations using Laplace transforms.

Module:7	**Application of Fourier series and Fourier transforms in Circuit Analysis**	**8 hours**

Trigonometric Fourier series, Symmetry conditions, Applications in circuit solving, Fourier transforms. Properties, Applications in circuit solving, Comparisons of Fourier and Laplace transforms.

Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**60 hours**

Text Book(s)	
1.	Charles K. Alexander, Matthew N. O. Sadiku, "Fundamentals of Electric Circuits," 2020, Seventh Edition, McGraw Hill Higher Education.
Reference Books	
1.	W.H.Hayt, J.E.Kemmerly & S.M.Durbin, "Engineering Circuit Analysis", 2019, Ninth Edition, McGraw Hill Higher Education.
2.	Allan R. Hambley, "Electrical Engineering – Principles & applications", 2016, Sixth Edition, Pearson Education, Noida, India.

Mode of Evaluation: Internal Assessment (CAT, Quizzes, Digital Assignments) & Final Assessment Test (FAT)

Recommended by Board of Studies	09-11-2021		
Approved by Academic Council	No. 64	Date	16-12-2021

Course Code	Course Title	L	T	P	C
BEVD101L	Electronic Materials	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

This course is aimed to:

1. Give the students a solid background, in relevant concepts, principles, and properties of electronic materials which are constituents of modern semiconductor devices.
2. Understand and comprehend basic materials physics and materials properties and use them for device application.
3. Correlate electronic materials properties with the semiconductor device characteristics.

Course Outcomes

After completion of the course, the student will be able to:

1. Learn and understand the concept of crystal structures and their defects.
2. Know the classical and quantum theory of materials.
3. Learn and understand the optical and thermal properties of materials.
4. Know the dielectric, ferroelectric, and magnetic properties of materials.
5. Understand the concept of superconductivity in materials.
6. Gain knowledge about various kinds of nanomaterials.

Module:1	Crystal structures, Defects	6 hours

Crystal system and Bravais lattices -Crystal structures Crystallographic planes and directions - Defects and imperfection in crystals - Analysis of crystal structures - X-ray diffraction - Bragg's law, Reciprocal lattice, Amorphous solids.

Module:2	Classical theory of materials	6 hours

Drude-Lorentz Classical free electron theory of metals, electrical conductivity, relaxation time, drift velocity, Matthiessen's rule, Temperature dependence of resistivity, Thermal conductivity, Wiedemann-Franz law, drawbacks of classical theory, Hall effect - theory - experimental proof; Hall Sensors.

Module:3	Quantum Theory of Materials	8 hours

Need for quantum mechanics, Schrodinger equation - Tunnel barrier, Electronic structure of H atom, Harmonic oscillator - H_2 molecule, Electronic Band structure - free electron band, electron in a one-dimensional potential well, Bloch theorem, Kronig-Penny Model, k-space, Brillouin Zone, Fundamentals of Metals, semiconductors and insulators (properties of materials useful for device application), Fermi-Dirac statistics, Fermi energy, Fermi Surface, effective mass. Electronic band models (E-k diagram) of representative metals, semiconductors and insulators, Density of states. Electrons, holes, excitons.

Module:4	Thermal & Optical properties of Materials	6 hours

Lattice vibrations - Harmonic oscillator and lattice waves, Phonons and Thermal properties: Monatomic, diatomic harmonic crystals, phonons, sound velocity, Heat Capacity - Debye model - Phonon density of states, Einstein model. Optical Properties - Photoconductivity, Optical absorption and transmission, Photoluminescence, Electroluminescence.

Module:5	**Dielectric, Ferroelectric, Piezoelectric, & Magnetic properties of materials**	**7 hours**
Insulators & Dielectric materials, Polarization, Clausius - Mosotti relation, Dielectric constant, Temperature & frequency dependence of dielectric constant, Dielectric loss, breakdown. Ferroelectric and Piezoelectric materials, and their applications in devices. Magnetic parameters and their relations - Origin of magnetization - orbital magnetic moment, spin magnetic moment, Bohr magneton, Properties (Qualitative description) of dia, para, antiferro and ferromagnetic materials - Domain theory of ferromagnetism, Hysteresis, applications.		
Module:6	**Superconductivity**	**5 hours**
Superconductors, types, properties, Meissner Effect - Effect of Magnetic Field - Critical Current Superelectrons - electrodynamics of Superelectrons - Penetration depth - BCS theory - Josephson Effect - Applications - SQUID.		
Module:7	**Nanomaterials**	**5 hours**
Fundamentals of Quantum wells, Quantum wires, Quantum dots and their applications.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**

Text Book(s)	
1.	Safa O. Kasap, Principles of Electronic Materials and Devices, 2018, 4th Edition, McGraw-Hill Education.
2.	Rolf E. Hummel, Electronic Properties of Materials, 2014, 4th Edition, Springer.
Reference Books	
1.	David Jiles, Introduction to the Electronic Properties of Materials, 2017, 2nd Edition, CRC Press.
2.	Manijeh Razeghi, Fundamentals of Solid-State Engineering, 2019, 4th Edition, Springer.
3.	Charles Kittel, Introduction to Solid-State Physics, 2019, 8th Edtion, Wiley India.
4.	M. A. Wahab, Solid State Physics - Structure and Properties of Materials, 2021, 3rd Edition, Narosa Publishing House.
5.	Paul Harrison and Alex Valavanis, Quantum Wells, Wires and Dots, 2016, 4th edition, John Wiley.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD201L	Physics of Semiconductor Devices	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

This course is aimed to:

1. Give the students in-depth knowledge of the physics of solid-state devices.
2. Impart the fundamentals of semiconductor devices, their structures, and operation.
3. Teach the modeling of PN Junction, MOS capacitors, and MOSFETs.
4. Introduce transistor scaling, short channel effects and alternate transistor technologies.
5. Gain full confidence to work with various semiconductor devices and their applications in discrete and integrated circuits.

Course Outcomes

After completion of the course, the student will be able to:

1. Apply the concepts of semiconductor energy band model and carrier transport.
2. Analyze the PN Junction diode characteristics.
3. Understand the principles of optoelectronic devices.
4. Evaluate the BJT characteristics and equivalent circuits from the device parameters.
5. Understand and derive the MOS capacitor characteristics.
6. Design the MOSFET with the required characteristics.

Module:1	Semiconductor Fundamentals	8 hours

Semiconductor materials, Basic Crystal Structure, Directions and planes in crystals, Formation of energy bands – E-k diagram, Effective mass – Concept of hole, Direct and indirect band gap, Density of states, Fermi-Dirac distribution, Fermi level, Intrinsic and extrinsic semiconductors, Equilibrium carrier concentration, Concept of Equilibrium, Non-equilibrium and Steady state, Excess Carriers, Electron-hole pair creation by radiation, Carrier lifetime, Quasi equilibrium and quasi-Fermi level. Generation and recombination of carriers – Excess carrier Lifetime, Semiconductor in electric field. Carrier drift, Mobility and velocity saturation, Carrier diffusion, Einstein's relation, Poisson equation, Continuity equation, Quantum tunneling.

Module:2	PN Junction	8 hours

PN Junction – Thermal Equilibrium Energy band diagram – Contact potential and space charge layers – Poisson equation – Electric fields and Potentials, PN junction under applied bias – Energy band diagrams – One-sided PN junction – Avalanche and Zener breakdown, Zener diode. Diode capacitances, small signal model of PN junction, Static current-voltage characteristics of PN junctions, Varactor diode, Heterojunctions. Metal-Semiconductor Contacts: Schottky, and Ohmic contacts, tunnel diodes, IMPATT diode

Module:3	Optoelectronic Devices	5 hours

Principles of operations of devices: Photo Diodes, Solar Cells, Light Emitting Diodes, Semiconductor LASERs.

Module:4	**Transistors**	**6 hours**
Bipolar Junction Transistors: Device structure and physical operation, current-voltage relationship – Common Base, Common Emitter configurations – Base width modulation; small signal and equivalent circuit models, Heterojunction Bipolar Transistors, Junction Field Effect Transistor, MESFET, MODFET (HEMT).		
Module:5	**MOS Capacitor**	**5 hours**
Ideal and realistic MOS Capacitors: Contact potential – Gate work function, Energy-band diagrams, Flat-band condition, Oxide and Interface charges, Accumulation, Depletion, Inversion, Strong inversion, Threshold voltage calculation, Body effect, Capacitance-voltage characteristics.		
Module:6	**MOSFET**	**7 hours**
MOSFET Physics: Surface Mobility, Drain current, Saturation voltage, Current-voltage characteristics, leakage currents, Small signal model – Short channel effects – Velocity saturation, Channel length modulation, Sub-threshold conduction – V_t roll-off, Drain-induced barrier lowering, Punch-through – Hot carrier degradation, Gate induced drain leakage, Gate leakage.		
Module:7	**MOSFET Scaling and Advanced Technologies**	**4 hours**
Scaling limits, alternative technologies – SOI MOSFET, multigate FETs		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**

Text Book(s)	
1.	Ben G Streetman, Sanjay Kumar Banerjee, Solid State Electronic Devices, 2015, 7th Edition, Pearson Education
2.	S. M. Sze and Kwok K Ng, Physics of Semiconductor Devices, 2021, 4th Edition, Wiley.
Reference Books	
1.	Donald A. Neamen, Semiconductor Physics and Devices, 2011, 4th Edition, McGraw Hill.
2.	S. M. Sze, M. K. Lee, Semiconductor Devices, 2015, 3rd Edition, John Wiley.
3.	Pallab Bhattacharya, Semiconductor Optoelectronic Devices, 2017, 2nd Edition, Pearson Education.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BECE102L	Digital Systems Design	3	0	0	3
Pre-requisite	Nil	Syllabus version			
		1.0			

Course Objectives

1. Provide an understanding of Boolean algebra and logic functions.
2. Develop the knowledge of combinational and sequential logic circuit design.
3. Design and model the data path circuits for digital systems.
4. Establish a strong understanding of programmable logic.
5. Enable the student to design and model the logic circuits using Verilog HDL.

Course Outcome

At the end of the course the student will be able to

1. Optimize the logic functions using and Boolean principles and K-map.
2. Model the Combinational and Sequential logic circuits using Verilog HDL.
3. Design the various combinational logic circuits and data path circuits.
4. Analyze and apply the design aspects of sequential logic circuits.
5. Analyze and apply the design aspects of Finite state machines.
6. Examine the basic architectures of programmable logic devices.

Module:1	Digital Logic	8 hours

Boolean Algebra: Basic definitions, Axiomatic definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Simplification of Boolean functions. Gate-Level Minimization: The Map Method (K-map up to 4 variable), Product of Sums and Sum of Products Simplification, NAND and NOR Implementation. Logic Families: Digital Logic Gates, TTL and CMOS logic families.

Module:2	Verilog HDL	5 hours

Lexical Conventions, Ports and Modules, Operators, Dataflow Modelling, Gate Level Modelling, Behavioural Modeling, Test Bench.

Module:3	Design of Combinational Logic Circuits	8 hours

Design Procedure, Half Adder, Full Adder, Half Subtractor, Full Subtractor, Decoders, Encoders, Multiplexers, De-multiplexers, Parity generator and checker, Applications of Decoder, Multiplexer and De-multiplexer. Modeling of Combinational logic circuits using Verilog HDL.

Module:4	Design of data path circuits	6 hours

N-bit Parallel Adder/Subtractor, Carry Look Ahead Adder, Unsigned Array Multiplier, Booth Multiplier, 4-Bit Magnitude comparator. Modeling of data path circuits using Verilog HDL.

Module:5	Design of Sequential Logic Circuits	8 hours

Latches, Flip-Flops - SR, D, JK & T, Buffer Registers, Shift Registers - SISO, SIPO, PISO, PIPO, Design of synchronous sequential circuits: state table and state diagrams, Design of counters: Modulo-n, Johnson, Ring, Up/Down, Asynchronous counter. Modeling of sequential logic circuits using Verilog HDL.

Module:6	Design of FSM	4 hours

Finite state Machine(FSM):Mealy FSM and Moore FSM , Design Example : Sequence detection, Modeling of FSM using Verilog HDL.

Module:7	Programmable Logic Devices	4 hours

Types of Programmable Logic Devices: PLA, PAL, CPLD, FPGA Generic Architecture.

Module:8	**Contemporary issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Textbook(s)	
1.	M. Morris Mano and Michael D. Ciletti, Digital Design: With an Introduction to the Verilog HDL and System Verilog, 2018, 6th Edition, Pearson Pvt. Ltd.
Reference Books	
1.	Ming-Bo Lin, Digital Systems Design and Practice: Using Verilog HDL and FPGAs, 2015, 2nd Edition, Create Space Independent Publishing Platform.
2.	Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, 2009, 2nd edition, Prentice Hall of India Pvt. Ltd.
3.	Stephen Brown and ZvonkoVranesic, Fundamentals of Digital Logic with Verilog Design, 2013, 3rd Edition, McGraw-Hill Higher Education.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	14-05-2022		
Approved by Academic Council	No. 66	Date	16-06-2022

Course Code	Course Title	L	T	P	C
BECE102P	Digital Systems Design Lab	0	0	2	1
Pre-requisite	Nil	Syllabus version			
		1.0			

Course Objective

- To apply theoretical knowledge gained in the theory course and get hands-on experience of the topics.

Course Outcome

At the end of the course the student will be able to

1. Design, simulate and synthesize combinational logic circuits, data path circuits and sequential logic circuits using Verilog HDL.
2. Design and implement FSM on FPGA.
3. Design and implement small digital systems on FPGA.

Indicative Experiments

1.	Characteristics of Digital ICs, Realization of Boolean expressions	**2 hours**
2.	Design and Verilog modeling of Combinational Logic circuits	**4 hours**
3.	Design and Verilog modeling of various data path elements - Adders	**2 hours**
4.	Design and Verilog modeling of various data path elements - Multipliers	**2 hours**
5.	Implementation of combinational circuits – (FPGA / Trainer Kit)	**2 hours**
6.	Implementation of data path circuit - (FPGA / Trainer Kit)	**2 hours**
7.	Design and Verilog modeling of simple sequential circuits like Counters and Shift registers	**2 hours**
8.	Design and Verilog modeling of complex sequential circuits	**2 hours**
9.	Implementation of Sequential circuits - (FPGA / Trainer Kit)	**2 hours**
10.	Design and Verilog modeling of FSM based design – Serial Adder	**2 hours**
11.	Design and Verilog modeling of FSM based design – Traffic Light Controller / Vending Machine	**4 hours**
12.	Design of ALU	**4 hours**
	Total Laboratory Hours	**30 hours**

Mode of Assessment: Continuous Assessment and Final Assessment Test			
Recommended by Board of Studies	14-05-2022		
Approved by Academic Council	No. 66	Date	16-06-2022

Course Code	Course Title	L	T	P	C
BECE204L	**Microprocessors and Microcontrollers**	**3**	**0**	**0**	**3**
Pre-requisite	**BECE102L**	**Syllabus version**			
		1.0			

Course Objectives:

1. To acquaint students with architectures of Intel microprocessors, microcontroller and ARM processors.
2. To familiarize the students with assembly language programming in 8051 microcontroller and ARM processor.
3. To interface peripherals and I/O devices with the 8051 microcontroller.

Course Outcome:

At the end of the course, the student should be able to

1. Comprehend the various microprocessors including Intel Pentium Processors
2. Infer the architecture and Programming of Intel 8086 Microprocessor.
3. Comprehend the architectures and programming of 8051 microcontroller.
4. Deploy the implementation of various peripherals such as general purpose input/ output, timers, serial communication, LCD, keypad and ADC with 8051 microcontroller
5. Infer the architecture of ARM Processor
6. Develop the simple application using ARM processor.

Module:1	Overview of Microprocessors	3 hours

Introduction to Microprocessors, 8-bit/16-bit Microprocessor, Overview of Intel Pentium, I (i3, i5, i7) Series Processor.

Module:2	Microprocessor Architecture and Interfacing: Intel x86	8 hours

16-bit Microprocessor: 8086 - Architecture and Addressing modes, Memory Segmentation, Instruction Set, Assembly Language Processing, Programming with DOS and BIOS function calls, minimum and maximum mode configuration, Programmable Peripheral Interface (8255), Programmable Timer Controller (8254), Memory Interface to 8086.

Module:3	Microcontroller Architecture: Intel 8051	7 hours

Microcontroller 8051 - Organization and Architecture, RAM-ROM Organization, Machine Cycle, Instruction set: Addressing modes, Data Processing - Stack, Arithmetic, Logical; Branching – Unconditional and Conditional, Assembly programming.

Module:4	Microcontroller 8051 Peripherals	5 hours

I/O Ports, Timers-Counters, Serial Communication and Interrupts.

Module:5	I/O interfacing with Microcontroller 8051	7 hours

LCD, LED, Keypad, Analog-to-Digital Convertors, Digital-to-Analog Convertors, Sensor with Signal Conditioning Interface.

Module:6	ARM Processor Architecture	5 hours

ARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.

Module:7	ARM Instruction Set	8 hours

ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI Instruction, Loading instructions, conditional Execution, Assembly Programming.

Module:8	Contemporary issues	2 hours

	Total Lecture hours:		**45 hours**
Text Book(s)			
1.	A.K. Ray, K.M. Bhurchandi, Advanced Microprocessor and Peripherals, 2012, 2nd Edition, Tata McGraw-Hill, India.		
2.	Mohammad Ali Mazidi, Janice G. Mazidi, Rolin D. McKinlay, The 8051 Microcontroller and Embedded Systems, 2014, 2nd Edition, Pearson, India.		
Reference Books			
1.	Muhammad Ali Mazidi, ARM Assembly Language Programming & Architecture: 1, 2016, 2nd Edition, Microdigitaled.com		
2.	A. Nagoor Kani, 8086 Microprocessors and its Applications, 2017, Second Edition, Tata McGraw-Hill Education Pvt. Ltd., New Delhi, India.		
3.	Joseph Yiu, The Definitive Guide to ARM® Cortex®-M0 and Cortex-M0+ Processors, 2015, 2nd Edition, Elsevier Science & Technology, UK		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	14-05-2022		
Approved by Academic Council	No. 66	Date	16-06-2022

Course Code	Course Title	L	T	P	C
BECE204P	Microprocessors and Microcontrollers Lab	0	0	2	1
Pre-requisite	BECE102L	Syllabus version			
		1.0			

Course Objectives

1. To familiarize the students with assembly language programming using microprocessor and microcontroller.
2. To familiarize the students with Embedded C language programming using microcontroller.
3. To interface peripherals and I/O devices with the microcontroller and microprocessor.

Course Outcome

Student will be able to

1. Showcase the skill, knowledge and ability of programming microcontroller and microprocessor using its instruction set.
2. Expertise with microcontroller and interfaces including general purpose input/ output, timers, serial communication, LCD, keypad and ADC.

Indicative Experiments [Experiments using 8086/8051/ARM]

1	Assembly language programming of Arithmetic/logical operations.	**6 hours**
2	Assembly language programming of memory operations.	**4 hours**
3	Assembly language programming/ Embedded C programming for interfacing the peripherals: General purpose input/ output, timers, serial communication, LCD, keypad and ADC.	**10 hours**
4	Hardware implementation of peripheral interfacing: General purpose input/ output, timers, serial communication, LCD, keypad and ADC.	**10 hours**
	Total Laboratory Hours	**30 hours**

Mode of Assessment: Continuous Assessment and Final Assessment Test			
Recommended by Board of Studies	14-05-2022		
Approved by Academic Council	No. 66	Date	16-06-2022

Course Code	Course Title	L	T	P	C
BECE302L	Control Systems	2	1	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

1. To study the use of transfer function model for the analysis of physical systems and to introduce the components of control system.
2. To provide adequate knowledge in the time response of systems and steady state error analysis along with the understanding of closed-loop and open-loop system analysis in frequency domain.
3. To introduce the design of controllers and compensators for the stability analysis.
4. To introduce state variable representation of physical systems and study the stability analysis in state space approach.

Course Outcomes

Students will be able to

1. Differentiate between open-loop and closed-loop control systems and obtain the transfer function from the mathematical modeling of physical systems.
2. Determine transient and steady state responses of the system with first and second order and also to analyze its error coefficients.
3. Characterize the system stability using R-H criteria and root locus techniques.
4. Analyze the frequency domain response of the control systems.
5. Design the controllers and compensators to estimate the system stability.
6. Analyze the system in state space model through the concept of controllability and observability.

Module:1	Control Systems	3 hours

Basic components of a control system, Applications, Open-loop control system and closed-loop control system, Examples of control system (air conditioner, cruise control, phase-locked loop, etc.), Effects of feedback on overall gain, Types of feedback control system, Linear and non-linear control systems.

Module:2	Mathematical Modeling of Physical Systems	8 hours

Difference and differential equations for LTI SISO and MIMO systems, Mathematical modeling of electrical and mechanical systems, Equivalence between the elements of different types of systems, Transfer function of linear systems, Open-loop transfer function and closed-loop transfer function, Block diagram representation, Block diagram reduction techniques, Signal flow graph using Mason's gain formula.

Module:3	Time Domain Response	6 hours

Transient response and steady state responses, Time domain specifications, Types of test inputs, Response of first order and second order systems, Steady state error, Static error coefficients, Generalized error coefficients.

Module:4	Characterization of Systems	5 hours

Stability – concept and definition, Poles, Zeros, Order and Type of systems; R-H criteria, Root locus analysis.

Module:5	Frequency Domain Response	7 hours

Frequency response – Performance specifications in the frequency domain, Phase margin and gain margin, Bode plot, Polar plot and Nyquist plot, Stability analysis in frequency domain.

Module:6	**Controllers and Compensators Design**	**7 hours**
Controllers – P, PI, PID, Realization of basic compensators, Cascade compensation in time domain and frequency domain, Feedback compensation, Design of lag, lead, lag-lead series compensators.		
Module:7	**State Space Analysis**	**7 hours**
Dynamic system modeling in state space representation: Diagonal canonical form, Jordan canonical form, Solutions of state equations of LTI system, Conversion from state space model to transfer function model and vice versa, Stability analysis in state spaces: Concept of eigenvalues and eigenvectors, State transition matrix using Cayley-Hamilton theorem, Controllability and observability.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Norman S. Nise, Control Systems Engineering, 2019, 8th Edition, John Wiley & Sons, New Jersey, USA
Reference Books	
1.	Farid Golnaraghi and Benjamin C. Kuo, Automatic Control Systems, 2017, 10th Edition, McGraw-Hill Education, India.
2.	I.J. Nagarth and M. Gopal, Control Systems Engineering, 2018, 6th Edition, New Age International Pvt. Ltd., New Delhi, India.
3.	Gene Franklin, J. Powell and Abbas Emami-Naeini, Feedback Control of Dynamic Systems, 2019, 8th Edition, Pearson Education, New Delhi, India.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	28-02-2023		
Approved by Academic Council	No. 69	Date	16-03-2023

Course Code	Course Title	L	T	P	C
BECE303L	VLSI System Design	3	0	0	3
Pre-requisite	BECE102L, BECE102P	Syllabus version			
		1.0			

Course Objectives :

1. To introduce the basic concepts and techniques of modern integrated circuit design.
2. Describe the fundamental principles underlying digital design using CMOS logic and analyze the performance characteristics of these digital circuits.
3. Verify that a design meets its functionality, timing constraints, both manually and through the use of computer-aided design tools.

Course Outcomes :

Students will be able to

1. Analyze the CMOS digital electronics circuits, including logic components and their interconnect using mathematical methods and circuit analysis models
2. Create models of moderately sized CMOS inverters with specified noise margin and propagation delay.
3. Apply CMOS technology-specific layout rules in the placement and routing of transistors and interconnect.
4. Analyse the various logic families and efficient techniques at circuit level for improving power and speed of combinational and sequential logic.
5. Implement the CMOS digital circuits with the specified timing constraints.
6. Design memories with efficient architectures to improve access times, power consumption

Module:1	VLSI Design Overview and MOSFET Theory	8 hours

VLSI Design Flow, Design Hierarchy, Concepts of Regularity, Modularity and Locality, VLSI Design Styles, Design Quality, MOSFET : Device Structure, Electrical behaviour of MOS transistors, Capacitance- Voltage Characteristics and Non-ideal Effects; Effects of scaling on MOSFETs and Interconnects.

Module:2	CMOS Logic Gates	8 hours

CMOS Inverter: DC Transfer Characteristics, Static and Dynamic Behaviour, CMOS Basic Gates, Compound Gates, CMOS Sequential Logic Design – Latches and Flip Flops

Module:3	CMOS Fabrication and Layout	5 hours

CMOS Process Technology N-well, P-well Process, latch up in CMOS technology, Stick Diagram for Boolean Functions using Euler Theorem, Layout Design Rule

Module:4	CMOS Circuits Performance Analysis	5 hours

Delay Estimation, Logical Effort and Transistor Sizing, Performance Estimation - Static & Dynamic Power Dissipation.

Module:5	CMOS Logic Families	8 hours

Pass Transistor Logic, Transmission Gates based Logic Design, pseudo NMOS, Cascode Voltage Switch Logic Dynamic and domino logic, clocked CMOS (C^2MOS) logic and np – CMOS logic.

Module:6	Timing Analysis	4 hours

Introduction to Static timing analysis, Setup Time, Hold Time, calculation of critical path, slack, setup and hold time violations.

Module:7	Semiconductor Memory Design	5 hours

Introduction, Types - Read-Only Memory (ROM) Circuits, Static Read-Write Memory (SRAM) and Dynamic Read-Write Memory (DRAM) Circuits.		
Module:8	**Contemporary issues**	**2 hours**
	Total Lecture Hours:	**45 hours**

Text Book(s)	
1.	Neil H.Weste, Harris, A. Banerjee, CMOS VLSI Design, A circuits and System Perspective, 2015, 4th Edition, Pearson Education, Noida, India.
Reference Book	
1.	Jan M. Rabaey, Anantha Chadrakasan, Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective Paperback, 2016, 2rd Edition, Pearson Education, India.
2.	Sung-Mo Kang, Yusuf Liblebici, Chulwoo Kim, CMOS Digital Integrated Circuits: Analysis and Design, 2019, Revised 4th Edition, Tata Mc Graw Hill, New Delhi, India.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	14-05-2022		
Approved by Academic Council	No. 66	Date	16-06-2022

Course Code	Course Title	L	T	P	C
BECE303P	VLSI System Design Lab	0	0	2	1
Pre-requisite	BECE102L, BECE102P	Syllabus version			
		1.0			

Course Objectives :

- The objective of this laboratory is to apply the theoretical knowledge and explore various design style of CMOS Integrated Circuits (IC) design using the latest EDA tools

Course Outcome :

On completion of this lab course the students will be able to

1. Analyze the performance of CMOS Inverter circuits on the basis of their operation and working.
2. Design the semiconductor memory cell, combinational, sequential and arithmetic circuit using CMOS design rules.
3. Construct layout of CMOS inverter, universal and basic logic gates.

Indicative Experiments

1	Parameter extraction for basic cell structure (NMOS and PMOS devices). • Analysis of MOS with width variation, body effect and estimation of channel length modulation	**2 hours**
2	Design and Analysis of CMOS inverter for arbitrary sizing. • Estimation of Power, Delay, Noise Margin. • Impact of load on performance metrics.	**4 hours**
3	Analysis of CMOS inverter for given specification. • Impact of sizing on Power, Delay, Noise Margin	**2 hours**
4	Analysis of inverter chains using progressive sizing to improve delay performance.	**2 hours**
5	Design and Analysis of Universal gates in static CMOS logic • Effect of input reordering.	**2 hours**
6	Design and Analysis of Boolean Expression (Simple Arithmetic Unit) in static CMOS logic.	**2 hours**
7	Design and Analysis of Pass transistor and Transmission gate based circuits	**4 hours**
8	Design and Analysis of CMOS sequential circuits (Latches and Flip Flops)	**4 hours**
9	Design a CMOS Memory cell (SRAM, DRAM) and verify its operation.	**4 hours**
10	Design Layout of CMOS inverter and perform post-layout analysis, DRC, Layout Vs. Schematic, Monte Carlo analysis, Corner analysis and etc.	**4 hours**
	Total Laboratory Hours	**30 hours**

Mode of Assessment: Continuous Assessment and Final Assessment Test			
Recommended by Board of Studies	14-05-2022		
Approved by Academic Council	No. 66	Date	16-06-2022

Course Code	Course Title	L	T	P	C
BEVD202L	Electromagnetic Field Theory	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

This course is aimed to:

1. Acquaint the students with basic concepts and properties of Electrostatics and magnetostatics.
2. Making the students understand the propagation of EM waves through time-varying Maxwell's equations and analyze the EM Wave propagation in different conducting and dielectric media.
3. Making the students comprehend the concept of transmission and reflection in various transmission lines and design different transmission lines using Smith chart

Course Outcomes:

After completion of the course, the student will be able to:

1. Evaluate and analyze Electric Fields and Electric Potential due to different Charge distributions.
2. Compute and analyze magnetic fields in different material media.
3. Understand the propagation of EM waves through time-varying Maxwell's equations
4. Comprehend the EM wave propagation in conducting as well as in dielectric materials.
5. Calculate the power of an EM wave while propagating through different materials.
6. Illustrate the wave mechanism in different transmission lines at high frequencies using transmission line parameters.

Module:1	Vector Analysis	5 hours

Cartesian coordinates: Vector Algebra - Vector Operations, Vector Algebra: Component Form, Triple Products, Position, Displacement, and Separation Vectors, How Vectors Transform. Differential Calculus: Gradient, Divergence, Curl, Product Rules, Second Derivatives. Integral Calculus: Line, Surface, and Volume Integrals. The Fundamental Theorem for Gradients, The Fundamental Theorem for Divergences, The Fundamental Theorem for Curls. Curvilinear Coordinates: Spherical Coordinates, Cylindrical Coordinates

Module:2	Electrostatics	8 hours

The Electric Field, Coulomb's Law, The Electric Field due to Continuous Charge Distributions (line, surface and volume charge), Field Lines, Flux, and Gauss's Law – The divergence of Electric field, Applications of Gauss's Law, The Curl of Electric field. Electric Potential, Poisson's Equation and Laplace's Equation, The Potential of a Localized Charge Distribution (line, surface, volume charge), Boundary Conditions, The Work It Takes to Move a Charge, The Energy of a Point Charge Distribution, The Energy of a Continuous Charge, Conductors: Basic Properties, Induced Charges, Surface Charge and the Force on a Conductor, Capacitors. Laplace's Equation in One, and Two Dimensions, Boundary Conditions and Uniqueness Theorems, Conductors and the Second Uniqueness Theorem, The

Method of Images: The Classic Image Problem, Induced Surface Charge, Force and Energy. Separation of Variables: Cartesian Coordinates, Spherical Coordinates. The Electric Field of a Dipole.		
Module:3	**Electric Fields in Matter**	**5 hours**
Electric Fields in Matter: Dielectrics, Induced Dipoles, Alignment of Polar Molecules, Polarization. The Field of a Polarized Object: Bound Charges, Physical Interpretation of Bound Charges, The Field Inside a Dielectric. The Electric Displacement: Gauss's Law in the Presence of Dielectrics, Boundary Conditions. Linear Dielectrics: Susceptibility, Permittivity, Dielectric Constant, Boundary Value Problems with Linear Dielectrics, Energy in Dielectric Systems, Forces on Dielectrics.		
Module:4	**Magnetostatics & Magnetic Fields in Matter**	**8 hours**
The Lorentz Force Law, Magnetic Fields, Magnetic Forces, Currents, The Biot-Savart Law, Steady Currents, The Magnetic Field of a Steady Current, Straight-Line Currents, The Divergence and Curl of B, Ampère's Law, Comparison of Magnetostatics and Electrostatics, The Vector Potential, Boundary Conditions. Magnetic Fields in Matter: Diamagnets, Paramagnets, Ferromagnets, Torques and Forces on Magnetic Dipoles, Effect of a Magnetic Field on Atomic Orbits, Magnetization. The Field of a Magnetized Object: Bound Currents, Physical Interpretation of Bound Currents, The Magnetic Field Inside Matter. The Auxiliary Field H, Ampère's Law in Magnetized Materials, Boundary Conditions. Linear Media: Magnetic Susceptibility and Permeability.		
Module:5	**Electrodynamics & Conservation Laws**	**5 hours**
Ohm's Law, Electromotive Force, Motional emf, Electromagnetic Induction, Faraday's Law, The Induced Electric Field, Inductance, Energy in Magnetic Fields, Electrodynamics Before Maxwell, How Maxwell Fixed Ampère's Law, Maxwell's Equations, Magnetic Charge, Maxwell's Equations in Matter, Boundary Conditions. Charge and Energy, The Continuity Equation, Poynting's Theorem, Newton's Third Law in Electrodynamics, Conservation of Momentum, Angular Momentum.		
Module:6	**Electromagnetic Waves**	**6 hours**
The Wave Equation, Sinusoidal Waves, Boundary Conditions: Reflection and Transmission, Polarization. Electromagnetic Waves in Vacuum: The Wave Equation for E and B, Monochromatic Plane Waves, Energy and Momentum in Electromagnetic Waves. Electromagnetic Waves in Matter: Propagation in Linear Media, Reflection and Transmission at Normal Incidence. Absorption and Dispersion: Electromagnetic Waves in Conductors, Reflection at a Conducting Surface.		
Module:7	**Transmission Lines & Smith Chart**	**6 hours**
Types, Parameters, Transmission Line Equations, Primary and secondary Constants, Expressions for Characteristic Impedance, Propagation Constant, Phase velocity, input impedance, Reflection Coefficient, VSWR. Characterization of lossless, low loss and distortionless transmission lines. Significance of short circuit and open circuit lines. Smith Chart and applications: Input impedance, admittance, VSWR, Reflection Coefficient, return loss, standing wave pattern.		

Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**
Text Book(s)		
1.	David. J. Griffiths, Introduction to Electrodynamics, 2020, Fourth edition, Cambridge University Press, India.	
2.	D. K. Cheng, Field and Wave Electromagnetics, 2014, Second edition, Pearson Education.	
Reference Books		
1.	D. K. Cheng, Fundamentals of Engineering Electromagnetics, 2014, Pearson India	
2.	Mathew N. O. Sadiku, and S. V. Kulkarni, Principles of Electromagnetics, 2015, Sixth edition, Oxford University Press.	
3.	Fawwaz T. Ulaby, Umberto Ravaioli, Fundamentals of Applied Electromagnetics, 2015, Pearson Global Edition.	
4.	William H. Hayt, J. A. Buck and M. Jaleel Akhtar, Engineering Electromagnetics, 2020, 9th Edition, McGraw Hill.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test		
Recommended by Board of Studies	03-11-2023	
Approved by Academic Council	No. 72	Date 13-12-2023

Course Code	Course Title	L	T	P	C
BEVD203L	Signal Processing	3	0	0	3
Pre-requisite	BMAT102L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Study the fundamentals like signal classification, signal operations and sampling techniques.
2. Study the different systems, convolution, and correlation.
3. Analyze different transform techniques and able to take the transform of a LTI system.
4. Inculcate the design concepts of digital FIR filters, analog and digital IIR Filters.
5. Instill diverse structures for realizing digital filters.
6. Provide an insight into digital signal processors.

Course Outcomes

After completion of the course the student will be able to:

1. Understand the fundamentals of signal classifications and the concept of sampling theorem.
2. Understand the different systems and concepts of convolution and correlation.
3. Apply the Fourier concepts to DT signals and Z transform to analyze the DT systems.
4. Comprehend the various analog filter design techniques and be able to design digital filters.
5. Realize the digital filters using various system interconnections.
6. Understand the types and architecture of digital signal processors.

Module:1	Continuous Time and Discrete Time Signals	6 hours

Representation of signals, Signal classification, Types of signals, Operations on signals - Scaling, Shifting, Transformation of independent variables, Norms and moments of signals, Sampling: Nyquist Criteria-Aliasing-Reconstruction

Module:2	Continuous Time and Discrete Time Systems	5 hours

Classification of systems - Static and dynamic, Linear and non-linear, Time-variant and time-invariant, Causal and non-causal, Stable and unstable, Impulse response and step response of systems, Convolution and Correlation for DT signals.

Module:3	Review of Transform Techniques	8 hours

Discrete Time System Analysis: Z-transform and its properties, inverse z-transforms; difference equation – Solution by z-transform, - Stability analysis.
Fourier Analysis of DT Signals: Review of Continuous-time Fourier transform and Discrete-time Fourier transform, DFT, Radix-2 FFT Algorithms.

Module:4	Design of Digital FIR Filters	7 hours

Design characteristics of FIR filters with linear- phase – Frequency response of linear phase FIR filters, Design of FIR filters using windowing techniques - Rectangular, Bartlett, Hamming, Hanning and Blackmann.

Module:5	Design of Digital IIR Filters	8 hours

Analog low pass filter -Butterworth and Chebyshev approximations. Different methods of IIR filter Design: Bilinear and Impulse invariance techniques.

Module:6	**Digital filter Structures**	**4 hours**
Basic FIR and IIR digital filter structures - Direct Forms, Cascade, Parallel, Lattice and Lattice-Ladder structures.		
Module:7	**Digital Signal Processors**	**5 hours**
General-purpose digital signal processors - Fixed point and floating-point DSP. Finite word length effect, Filter operation in different DSP Architectures, Typical implementation of DSP algorithms.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	John G. Proakis, Dimitris G Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, 2022, 5th Edition, Pearson, USA
2.	R.S.Kaler, M.Kulkarni, Umesh Gupta, A textbook of Digital Signal Processing, 2019, 1st edition, Dream tech Press, Wiley, India
Reference Books	
1.	P. Rama Krishna Rao and Shankar Prakriya, "Signals and Systems", 2017, 2nd edition - Mc-Graw Hill.
2.	Alan. V. Oppenheim, Alan. S. Willsk and S. Hamid Nawab, Signals and Systems, 2015, 2nd Edition, Pearson Education India.
3.	Keshab K. Parhi, "VLSI Digital Signal Processing Systems", 1999, Wiley Eastern.
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test	

Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD204L	Electronic Circuits	3	0	0	3
Pre-requisite	BEVD201L	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Introduce the relationship of BJT device and circuits.
2. Describe the fundamental principles underlying design of various building blocks and Amplifier circuits using BJT's and analyse their performance characteristics.
3. Understand op-amp performance characteristics and its applications.
4. Understand waveform generator and oscillators.

Course Outcomes:

At the end of the course the student will be able to

1. Understand the fundamentals of BJT Operation and apply them to design various building blocks.
2. Comprehend the various configurations of BJT Amplifiers and their characteristics.
3. Understand the fundamentals of op-amp and its various configurations.
4. Design and Analyse various Feedback Amplifiers.
5. Build op-amp based circuits to generate various waveforms.
6. Comprehend the design of op-amp based oscillators.

Module:1	Bipolar Junction Transistors (BJTs)	4 hours

Device Structure and Physical Operation-PNP/NPN Transistors and Modes of Operation, Current–Voltage Characteristics, BJT Circuits at DC, Transistor Breakdown and Temperature Effects.

Module:2	Bipolar Junction Transistor (BJT) Amplifiers	9 hours

Basic Principles- Basis, Obtaining Voltage Amplifier, VTC, Small-Signal Operation and Models, Basic Configurations-Common-Emitter, Common-Base, Common-Collector, Biasing in BJT, Frequency Response- Internal Capacitive Effects, Miller Theorem and the High-Frequency Model of BJT, Frequency Response of Common-Emitter amplifier, BJT Power Amplifiers- Class A, Class B, Class AB.

Module:3	Building Blocks of Integrated-Circuit Amplifiers	6 hours

Current Sources, Current Mirrors, and Current-Steering Circuits-BJT Circuits, BJT Cascode, Darlington Configuration, BJT Differential Pair-Basic Operation, Large/Small Signal Models, The Differential Amplifier with a Current-Mirror Load, Input Offset Voltage.

Module:4	Feedback Amplifiers	6 hours

General Feedback Structure, Properties of Negative Feedback, Determination of loop gain, Various Feedback Amplifier Topologies-Voltage Series, Voltage shunt, Current series, Current shunt.

Module:5	Operational Amplifiers	6 hours

Operational Amplifier as a Black Box-General Considerations and Op-Amp-Based Circuits-Inverting, Non-Inverting, Difference Amplifier, Differentiator, Integrator, Bipolar OpAmp- 741 BJT Circuit, DC/AC Analysis, Op Amp-Gain, Frequency Response, Slew Rate, Modern Techniques for the design of BJT Op Amps.		
Module:6	**Comparators and Waveform generators**	**8 hours**
Comparator, Schmitt trigger and its applications, Waveform Generators-Square Wave, Triangular etc., 555 timer- Astable, Monostable Multivibrators, Rectifier, Peak detector.		
Module:7	**Oscillators**	**4 hours**
Basic Principles of Oscillators, Op-Amp RC Oscillators-Phase Shift, Wein's Bridge.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R&D Organizations.		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Adel.S.Sedra & Kenneth C. Smith, Tony Carusone, Vincent Gaudet, Microelectronics Circuits, 2021, Eighth International Edition, , Oxford University Press, New York.
2.	Donald A.Neamann, Microelectronics: Circuit Analysis & Design, 2021, Fourth Edition, Mcgraw Hill, New York.
Reference Books	
1.	Behzaad Razavi, Fundamentals of Microelectronics, 2021, Third Edition, Wiley Publications, Hoboken, New Jersey.
2.	D Roy Choudhury, Shail B Jain, Linear integrated Circuits, 2021, Sixth Edition, New Age International, India.
3.	Albert P. Malvino, David J. Bates, Patrick E. Hoppe, Electronic Principles, 2021 Ninth Edition, McGraw Hill, Glencoe.
4.	Ramakant A. Gayakwad Op-Amps and Linear Integrated Circuits, 2015, Fourth Edition, Pearson education, India.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD204P	Electronic Circuits Lab	0	0	2	1
Pre-requisite	BEVD201L	Syllabus version			
		1.0			

Course Objectives:

The course is aimed to

1. Understand the design and analysis of various BJT based amplifier configurations.
2. Comprehensive study and analysis of op-amp and its various applications.

Course Outcomes:

At the end of the course the student will be able to

1. Design and analyze various BJT based amplifier configurations in a breadboard.
2. Understand the working of op-amp and its applications using breadboard / SPICE software.

Indicative Experiments (Following experiments will be done either hardware or software.)

1.	Study of Input/Output Characteristics of in CE/CC configurations.	2 hours
2.	Study of Input/Output Characteristics of BJT Power Amplifiers- Class A, B, AB.	2 hours
3.	Study of Characteristics of an NPN/PNP BJT based Differential Amplifier	2 hours
4.	Study of characteristics of an op-amp.	2 hours
5.	Op-amp as an Inverting and Non-Inverting Amplifier.	2 hours
6.	Voltage/Current Feedback amplifier using op-amp.	2 hours
7.	Op-amp as an Integrator and Differentiator Amplifier.	4 hours
8.	Op-amp as a Comparator and Schmitt Trigger.	2 hours
9.	Op-amp as Waveform Generator- Square Wave, Triangular etc. (Multivibrators)	4 hours
10.	Oscillator design using op-amp -Wein's Bridge, RC Phase Shift.	4 hours
11.	Design of 3-bit Flash ADC.	2 hours
12.	Design of active filters-Low pass, High pass.	2 hours
	Total Laboratory Hours	**30 hours**

Mode of assessment: Continuous Assessment Test and Final Assessment Test

Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD205L	Scripting Languages and Verification	3	0	0	3
Pre-requisite	BECE102L, BECE102P	Syllabus version			
		1.0			

Course Objectives

This course is aimed to:

1. Write Perl, TCL and Python scripts in the LINUX environment.
2. Write test bench using System Verilog.
3. Develop class based test bench using System Verilog.

Course Outcomes

After completion of the course the student will be able to:

1. Handle files, directories and manage processes using PERL scripts.
2. Handle files, directories and manage processes using TCL scripts.
3. Develop scripts for Automation.
4. Understand the VLSI Verification Techniques.
5. Develop System Verilog modules.
6. Develop System Verilog constrained random test environment.

Module:1	PERL	7 hours

Introduction – Scalar Data – Lists and Arrays – Control Structures - Subroutines – Input and Output – Hashes - Regular Expressions - Directory Operations – Process Management – Packages and Modules – Applications.

Module:2	TCL	6 hours

An Overview of TCL and Tk –Tcl Language syntax – Variables – Expressions – Lists – Control flow – procedures – Errors and exceptions – String manipulations – Accessing files- Processes. Applications – Controlling Tools – Basics of Tk – Applications.

Module:3	Verification Guidelines	4 hours

Verification Process – Basic Testbench Functionality – Directed Testing – Constrained Random Stimulus – Functional Coverage – Testbench Components – Layered Testbench - Code coverage – Functional coverage.

Module:4	System Verilog Basics	7 hours

Introduction to System Verilog – Literal values-data Types – Arrays – Array methods – Creating new types with typedef – user defined structures – Enumerated types – Packages – operators – expressions – Procedural statements and control flow – Processes in System Verilog – Task and functions – Routine arguments – Returning from a routine.

Module:5	Basic OOPS	6 hours

OOP Terminology - Creating Object - object deallocation - copying objects - static variables - Global variables – Inheritance – Polymorphism.

Module:6	Randomization	4 hours

Need for Randomization – Randomization in System Verilog – Constraint Details – Solution Probabilities – Controlling Multiple Constraint Blocks – Valid Constraints – In-line Constraints – Common Randomization Problems.		
Module:7	**Connecting Test bench and Design**	**9 hours**
Program – Interface - Stimulus timing - Module interactions - Connecting together - Development of self-checking test environment – Generator – Transactor – Driver – Monitor – Checker – Scoreboard.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total hours:	**45 hours**

Text Book(s)	
1.	Curtis Poe, Beginning Perl, 2012, First Edition, Wiley.
2.	Clif Flynt, Tcl/Tk A Developer's Guide, 2012, Third Edition, Elsevier.
3.	Ashok B. Mehta, Introduction to System Verilog, 202, First Edition, Springer.
Reference Books	
1.	Larry Wall, Tom Christiansen, John Orwant, Programming PERL, 2012, Fourth Edition, Oreilly Publications.
2.	John K. Ousterhout, Ken Jones, Tcl and the Tk Toolkit, 2010, Second Edition, Pearson Education.
3.	Christian B Spear, System Verilog for Verification: A guide to learning the Test bench language features, 2012, Third Edition, Springer publications.
4.	Quan Nguyen, CAD Scripting Languages: A collection of Perl, Ruby, Python, TCL & SKILL scripts, 2008, Ramacad.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD205P	Scripting Languages and Verification Lab	0	0	2	1
Pre-requisite	BECE102L, BECE102P	Syllabus version			
		1.0			

Course Objectives:

This course is aimed to:

1. Write Perl, TCL and Python scripts in the LINUX environment.
2. Write testbench using System Verilog.
3. Develop class based testbench using System Verilog.

Course Outcome:

After completion of the course the student will be able to:

1. Develop scripts for Automation.
2. Develop System Verilog constrained random test environment.

Indicative Experiments

1.	Write a script which reads a verilog design module and identifies whether it is a sequential or combinational design. Accordingly, the perl script should generate the testbench file in verilog. Also, the input vectors from the testbench should be in a randomized fashion.	6 hours
2.	Write a script that reads a set of log files from different simulation directories and generates a consolidated report in .xls format which should contain the information of the test name, status and error messages. If the test is indicated as successful in the log file, the status in the report should be as "TEST PASSED" and if the test is unsuccessful, then the report should display the status as "TEST FAILED".	4 hours
3.	Write a TCL Script which when executed should automatically compile your design modules and testbench modules and then perform the simulation. If the simulation is successful, then the script should synthesize the design module. The TCL script should also create a separate directory to dump the log files and a separate directory to write the netlist file.	4 hours
4.	Develop System Verilog task based Verification environment for a DUT (Router/APB/AHB).	8 hours
5.	Develop System Verilog class based Verification environment for a DUT (Router/APB/AHB).	8 hours
	Total Laboratory Hours	**30 hours**

Mode of Evaluation: Continuous Assessment and Final Assessment Test

Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD206L	Semiconductor Device Modelling	2	0	0	2
Pre-requisite	BEVD201L	Syllabus version			
		1.0			

Course Objectives

This course is aimed to:

1. Introduce students to TCAD simulation and Compact Modelling of Semiconductor Devices
2. Introduce the students to the fundamentals of Semiconductors and Device Physics and the operation of Junction Diodes and MOSFETs.
3. Introduce the students to SPICE models for MOSFETs and Diodes.
4. Introduce the students to multigate transistors (FINFETs) and their SPICE models e.g. BSIM-CMG and BSIM-IMG.

Course Outcomes

After completion of the course, the student will be able to:

1. Understand the semiconductor physics and carrier transport mechanism in semiconductors and model the P-N Junction Diode.
2. Understand the physics of MOSFETs and equivalent circuit models for MOSFETs
3. Understand Technology Computer-Aided Design (TCAD) tools and simulate the electrical characteristics of various semiconductor devices using these tools.
4. Understand the Compact modelling and model the MOSFETs using SPICE Level-1, Level-2, and Level-3 models.
5. Model the MOSFETs using industry-standard BISIM3 and BSIM4 MOSFET SPICE Models and FINFETs using BSIM CMG and BSIM IMG models.
6. Model the FINFETs using BSIM CMG and BSIM IMG models.

Module:1	**PN Junction Diode and Schottky Diode**	**5 hours**
Review of semiconductor Physics and Carrier transport in semiconductors, P-N Junction Diode-DC Current-Voltage Characteristics, P-N Diode-Static Model, Large-Signal Model, Small- Signal Model, SPICE Models of p-n diode.		
Module:2	**MOS Transistor Theory**	**4 hours**
MOS Transistor-Small signal modelling for low frequency and High frequency, Pao-Sah and Brews models; Short channel effects in MOS transistors, Narrow width effects, MOSFET scaling		
Module:3	**Introduction to TCAD Simulation**	**4 hours**
Introduction to Technology Computer-Aided Design (TCAD) tools, Carrier Transport Models-Drift Diffusion model, Energy Balance model, Hydrodynamic Model.		
Module:4	**Introduction to compact modelling**	**4 hours**
Introduction to compact modelling, Motivation for Compact Modelling, MOSFET-SPICE Level 1, Level 2 and Level 3 Models and model parameters.		
Module:5	**SPICE Models for Semiconductor Devices-I**	**6 hours**
SPICE Models for Semiconductor Devices: MOSFET- BSIM3 model parameters, BSIM CMG and BSIM IMG models.		
Module:6	**SPICE Models for Semiconductor Devices-II**	**3 hours**
SPICE Models for Semiconductor Devices: MOSFET- BSIM4 Model parameters		
Module:7	**Multigate FETs and FINFETs**	**2 hours**

Multigate transistors, FINFETs and GAA devices		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**30 hours**

Text Book(s)	
1.	B. G. Streetman and S. Banerjee, Solid State Electronic Devices, 2015, 7th Edition, PHI Private Limited.
2.	A. B. Bhattacharyya, Compact MOSFET Models for VLSI Design, 2009, Wiley.
3.	Chandan Kumar Sarkar, Technology Computer Aided Design: Simulation for VLSI MOSFET, 2018, CRC Press.
4.	T. A. Fjeldly, T. Ytterdal, and M. Shur, Introduction to Device Modelling and Circuit Simulation, 1998, John Wiley.
Reference Books	
1.	Donald A. Neamen, Semiconductor Physics, and Devices - Basic Principles, 2021, Indian Edition, McGraw Hill.
2.	R. F. Pierret, Semiconductor Device Fundamentals, 2006, Pearson.
3.	Samar K. Saha, Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond, 2017, 1st edition, CRC Press.
4.	G. Massobrio and P. Antognetti, Semiconductor Device ming with SPICE, 2010, 2nd Edition, TMH.
5.	Y. P. Tsividis, Operation, and Modelling of the MOS Transistor, 1987, McGraw-Hill.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test

Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD206P	Semiconductor Device Modelling Lab	0	0	2	1
Pre-requisite	BEVD201L	Syllabus version			
		1.0			

Course Objectives

This course is aimed to:

1. Introduce TCAD Simulation and SPICE modelling of Semiconductor Devices
2. Introduce with SPICE model parameter extraction for diodes.
3. Introduce with SPICE model parameter extraction for MOSFETs, and FINFETs

Course Outcomes

After completion of the course, the student will be able to:

1. Create device structure and simulate the device characteristics using TCAD tools.
2. Extract industry-standard SPICE models for diodes.
3. Extract industry-standard SPICE models for MOSFETs.

Indicative Experiments

1.	(i) Introduction to TCAD tools (ii) Creating p-n junction diode structure and simulating its I-V Characteristics using TCAD tools	4 hours
2.	Creating NMOS structure and simulation of I_D-V_{GS} and I_D-V_{DS} characteristics using TCAD tools and extraction of the following parameters (i) Threshold voltage extraction (ii) Subthreshold slop extraction (iii) DIBL extraction (iv) Body coefficient extraction (v) Substrate and gate current extraction (vi) Breakdown voltage extraction (vii) Short channel device current	4 hours
3.	FinFET structure creation and extraction of DC parameters and AC parameters	4 hours
4.	i) Introduction to SPICE tools ii) Level 1 Diode Model Extraction	2 hours
5.	MOSFET-SPICE level-1, Level-2 and Level-3 Model Extraction	4 hours
6.	MOSFET- BSIM3 MOSFET Model Extraction	4 hours
7.	MOSFET-BSIM-CMG and BSIM-IMG Model parameter extraction	4 hours
8.	BSIM4/BSIM-BULK MOSFET Model Extraction	4 hours
	Total Laboratory Hours	**30 hours**

Mode of Evaluation: Continuous Assessment and Final Assessment Test

Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD207L	Computer Architecture	3	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

This course is aimed to:

1. Learn the basic structure and operations of a computer.
2. Learn the arithmetic and logic unit and implementation of fixed-point and floating-point arithmetic units.
3. Understand parallelism and multi-core processors.
4. Understand the memory hierarchies, cache memories and virtual memories.

Course Outcomes:

After completion of the course the student will be able to:

1. Understand the basic structure of computers, operations, and instructions.
2. Understand the arithmetic and logic unit and implementation of fixed-point and floating-point arithmetic units.
3. Understand the various memory systems.
4. Understand the processor design control unit.
5. Understand parallel processing and pipelined execution.
6. Comprehend the methods of performance enhancement techniques such as pipelining and their hazards, Scalar and Vector processing architectures, and Multiprocessing techniques like SMP.

Module:1	Overview of Computer Architectures	5 hours

Organization vs. Architecture – Defining Computer Architecture, Flynn's Classification of Computers – Metrics for Performance Measurement – Von-Neumann vs. Harvard architectures.

Module:2	Arithmetic Operations in Computer	5 hours

Addition and Subtraction – Multiplication – Division – Floating Point Representation – Floating Point Operations.

Module:3	Memory Hierarchy Design	8 hours

Semiconductor memories – Memory cells – SRAM and DRAM cell, Cache memory unit – Concept of cache memory – Mapping methods – Organization of a cache memory unit – Fetch and write mechanisms, Memory management unit – Concept of virtual memory, Address translation.

Module:4	Processor Control Unit	6 hours

Machine instructions – Operands – Addressing modes – Instruction formats, Instruction set architectures – CISC and RISC architectures – Instruction Cycle, Control Unit – organization and operation of control Unit – Hardwired and Micro programmed control Unit.

Module:5	Instruction Level Parallelism	8 hours

Instruction-level Parallelism – Concepts and Challenges, Basic Compiler Techniques for Exposing ILP – Reducing Branch Costs with Advanced Branch Prediction – Dynamic Scheduling – Advanced Techniques for Instruction Delivery

and Speculation – Limitations of ILP, Multithreading-Exploiting Thread-Level Parallelism to Improve Uniprocessor Throughput.		
Module:6	**Thread Level Parallelism**	**6 hours**
Introduction, Shared-Memory Architecture – Performance Metrics for Shared-Memory Multicore Systems – Distributed Shared-Memory and Directory-Based Coherence, Cache Coherence Protocols – Synchronization – Memory Consistency.		
Module:7	**Data Level Parallelism**	**5 hours**
Vector architectures – SIMD architectures, Graphics Processing Units – Graphics processing units (GPUs) – GPU Memory Hierarchy, Detecting and Enhancing Loop Level Parallelism.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	J.L. Hennessy and D.A. Patterson, Computer Architecture: A Quantitative Approach, 2017, 6th Edition, Morgan Kauffmann.
2.	Harris, Sarah L., and David Harris, Digital design and computer architecture RISC-V Edition, 2021, Morgan Kauffmann.
Reference Books	
1.	Kirk DB and Wen-Mei WH, Programming massively parallel processors: a hands-on approach, 2022, 4th Edition, Morgan Kauffmann.
2.	David A. Patterson and John L. Hennessy, Computer Organization and Design RISC-V Edition, 2021, 2nd Edition, Morgan Kauffmann.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD301L	ASIC Design	3	0	0	3
Pre-requisite	BECE102L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Understand the RTL synthesis Flow with respect to different cost functions.
2. Understand the concepts of design for testability.
3. Analyse Static Timing requirements for ASIC design.
4. Discuss the guidelines at each abstraction level in physical design.
5. Understand the importance of physical design verification.

Course Outcomes

After completion of the course the student will be able to:

1. Synthesize the given design by considering various constraints and to optimize the same.
2. Perform the DFT techniques for the netlist.
3. Understand various timing parameters and perform Static Timing Analysis for ASIC design.
4. Compare OCV modelling techniques.
5. Perform physical design by adhering to guidelines.
6. Understand the importance of physical design verification.

Module:1	ASIC Design Methodology & Design Flow	4 hours

Implementation Strategies for Digital ICs - Custom IC Design- Cell-based Design Methodology - Array based implementation approaches - Traditional and Physical Compiler based ASIC Flow.

Module:2	RTL Synthesis	8 hours

RTL synthesis Flow – Review of RTL Coding style - Synthesis Design Environment & Constraints – Architecture of Logic Synthesizer - Technology Library Basics– Components of Technology Library –Synthesis Optimization- Technology independent and Technology dependent synthesis- Formal Verification – LEC.

Module:3	Design for Testability	5 Hours

Fault Models - Fault Simulation - Test Generations- ATPG - Design for Testability Scan based testing and logic BIST.

Module:4	Basic Static Timing Analysis	7 hours

Timing Parameter Definition – Setup Timing Check- Hold Timing Check- Multicycle Paths- Half-Cycle Paths- False Paths – Clock Gated Path.

Module:5	Advanced Static Timing Analysis	5 hours

Clock skew optimization – On-Chip Variations- AOCV-POCV-Time Borrowing- Setup and Hold Violation Fixing, Clock Domain Crossing (CDC) – Synchronization Techniques.

Module:6	Physical Design	8 hours

Detailed steps in Physical Design Flow- Guidelines for Floor plan, Placement, CTS

and routing– ECO flow – Signal Integrity Issues – CrossTalk - Timing Closure Techniques.		
Module:7	**Physical Design Verification**	**6 hours**
Timing Sign-off, Physical Verification – Sign-off DRC and LVS, ERC, IR Drop Analysis, Antenna Checks, Electro-Migration Analysis and ESD Analysis.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total hours:	**45 hours**

Text Book(s)	
1	Vaibbhav Taraate, ASIC Design and Synthesis RTL Design Using Verilog, 2021, 1st Edition, Springer, Singapore.
2	J. Bhasker and Rakesh Chadha, Static Timing Analysis for Nanometer Designs, 2010, 1st Edition, Springer, USA.
3	Andrew B. Kahng, VLSI Physical Design: From Graph Partitioning to Timing Closure, 2022, 2nd Edition, Springer.
Reference Books	
1	Khosrow Golshan, Physical Design Essentials: An ASIC Design Implementation Perspective, 2010, 1st Edition, Springer.
2	Michael John Sebastian Smith, Application-Specific Integrated Circuits, 2010, 1st Edition, Addison Wesley.
3	M. Bushnell, Vishwani Agrawal - Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, 2006, 1st Edition, Springer.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD301P	ASIC Design Lab	0	0	2	1
Pre-requisite	BECE102L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Apply theoretical knowledge gained in the ASIC Design course and get hands-on experience of the topics.

Course Outcomes

At the end of the course the student will be able to:

1. Design, simulate and synthesize complex digital system.
2. Analyse and fix the timing violations.
3. Design ASIC based digital systems using industry standard EDA tools.

	Indicative Experiments (For Complex Designs)	
1.	Design of Digital Architecture for given specification Develop an architecture for simple bidirectional 2-wire bus for efficient inter-IC control, called the Inter-IC or I2C bus. Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Serial, 8-bit oriented, bidirectional data transfers can be made at up to 100 kbit/s in Standard-mode, up to 400 kbit/s in Fast-mode.	**4 hours**
2.	Logical Synthesis of Digital Architecture Defining the RTL synthesis for technology specific libraries, design rule constraints and design optimization constraints. Given that you have RVT, LVT, LVT cell flavors available, what all flavors of cells do you want to use for synthesis. Along with DFT techniques. After running synthesis, suppose you are seeing lot of setup (max_delay) timing violations, how will you debug. What could be the reasons for the violations.	**8 hours**
3.	Netlist Optimization and GLS and Formal Verification The basic strategies are design parameter-oriented optimization (timing, power, area). For hierarchical designs bottom-up and top-down strategies to be applied. In this lab timing, power and area focused optimization strategies are applied.	**6 hours**
4.	Physical Synthesis of Digital Architecture i) Create a floorplan such that Utilization of the core area of the design is 40% - 60%. Die-edge to core-edge space is equal to the 1um Place all ports on left edge of the floor planned design in M4/M5 layers (based on preferred direction) and change the placement status of the ports to fixed. Place all macros following all floorplan guidelines Put power mesh in top two layers connected to the std-cell rails. Let the width of straps be 1um and set-to-set spacing at 7um. ii) Create a placement such that Insert End-cap cells, tap-cells, IO port buffers. Place tap cells such that on every row, nwell/pwell will be tied to pwr/gnd respectively at no farther than 17um.	**8 hours**

	Place the design using congestion driven placement with high effort as the option. Perform global route if tool has not done this already. iii) Perform the optimization such that Apply below flat derates for both net and cell and dump timing report with paths having slack worse than -100ps with the report having derates, input transition, nets as options. Keep the report in assignment. a) Late = 7% b) Early = 5% Reset the above applied derates and now dump a timing report with paths having slack worse than -100ps with the report having derates, input transition, nets as options. Keep the report in assignment. if any DRC and timing violations, try to fix manually and give the report. iv) Perform a CTS and routing after CTS such that You will have to do 2 different CTS experiments (Only clock tree synthesis and clock routing to be done. No timing optimization to be done) using the placed database you used in your lab. For each of the experiments, use M6 & M7 as clock routing layers. Clock cells to be used in each case/experiment are given below. Case 1: Use only clock INVERTER cells with all drive strengths and route the clock tree with double width and double-spacing routing rules. Case 2: Use only clock BUFFER cells with all drive strengths and route the clock tree with double width and triple spacing routing rules.	
5.	Physical Verification of Digital Architecture Timing ECO Flow report _analysis_coverage in both corners with parasitics (.spef) report _analysis_coverage in both corners with parasitics (.spef) after fixing violations timing_eco script to fix violations report_qor after place and route using timing_eco. if any DRC and timing violations, try to fix manually and give the report.	**4 hours**
	Total Laboratory Hours	**30 hours**

Mode of Assessment: Continuous Assessment Test and Final Assessment Test			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD302L	Principles of Communication Systems	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Explore the basic building blocks of analog and digital communication systems.
2. Explain the need for modulation and describe the concepts of amplitude and angle modulation schemes.
3. Understand the concepts of baseband and passband communication.
4. Apply source Coding and Channel Coding techniques in digital communication.

Course Outcomes

After completion of the course the student will be able to:

1. Comprehend the elements of electronic communication systems.
2. Understand the concepts of amplitude modulation and angle modulation.
3. Comprehend the sampling and quantization process to recover the original signal.
4. Analyze the performance of various waveform and Line coding techniques.
5. Analyze various passband communication techniques.
6. Examine various source coding and channel coding techniques.

Module:1	Introduction to Communication Systems	5 hours

Block diagram of communication system, Types of Communication systems, Modulation – Need for modulation- Types of modulation -Electromagnetic Spectrum for communication systems, Concept of bandwidth, Introduction to Noise and its types, Signal-to-Noise ratio, Noise Figure.

Module:2	Amplitude Modulation	6 hours

Elements of Analog Communication System-Amplitude Modulation (AM) – frequency spectrum of AM– Power in AM wave – Generation of AM signal. AM demodulation - Envelope detector and Coherent detector.

Module:3	Angle Modulation	6 hours

Principle of Frequency Modulation (FM) and Phase Modulation (PM) – Relation between FM and PM – Frequency Spectrum of FM – Transmission Bandwidth of FM– Narrow band and Wide band FM. Generation of FM- Direct method -Indirect Method. FM detectors – Phase discriminators – Ratio detectors - Phase Locked Loop (PLL). Pre-emphasis and De-emphasis.

Module:4	Baseband Digital Transmission	7 hours

Elements of Digital Communication System - Sampling –Types of sampling, Nyquist rate, Quantization, Encoding, Pulse Digital Modulation Techniques- PCM, DPCM, and DM. Introduction to Line coding techniques and types, Representation of line codes – Unipolar, Polar, Bipolar using NRZ and RZ, Manchester, Polar Quaternary codes, Differential encoding, Properties and applications of line codes.

Module:5	Passband Digital Communication	7 hours

Digital modulation Techniques- Advantages of Digital modulation Techniques over Analog modulation schemes, Generation and Detection of various digital modulation

schemes - ASK, FSK, PSK, QPSK. Comparison of Binary and M-ary modulation techniques.		
Module:6	**Source Coding**	**6 hours**
Shannon's information capacity theorem, Source coding theorem. Data compression using Shannon Fano coding and Huffman coding.		
Module:7	**Channel Coding**	**6 hours**
Channel Coding Theorem. Error control coding: Linear Block codes, Cyclic Codes, Convolutional Codes- Code tree, State diagram.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Kennedy," Electronic Communication Systems", 2011, 5th Edition, Mc Graw Hill Publications.
2.	Simon Haykin, Digital Communications, 2013, 1st Edition, John Wiley, India.
Reference Books	
1.	Bernard Sklar and Fredric J. Harris "Digital Communications – Fundamentals and applications", 2020, Third Edition, Pearson.
2.	Simon Haykins, Michael Moher," Introduction to Analog and Digital Communications", 2006, Second Edition, Wiley.
3.	K.Sam Shanmugam," Digital and Analog Communication Systems", 2012, Wiley.
4.	Hwei Hsu, Debjani Mitra, "Analog and Digital Communications", Schaum series, 2009, Tata McGraw Hill Education Private Limited.
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test	

Recommended by Board of Studies	03-11-2023		
Approved by Academic Council	No. 72	Date	13-12-2023

Course Code	Course Title	L	T	P	C
BEVD303L	CAD for IC Design	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Provide the fundamentals of graph theory, graph algorithms and their application to VLSI design automation and basic understanding of computational complexity of algorithms.
2. Comprehensive understanding of algorithms related to partitioning, chip planning, placement, routing of modules and clock signal and provide basic understanding of timing-driven placement, routing and physical synthesis.
3. Provide basics of the use of machine learning in VLSI computer aided design.

Course Outcomes

At the end of the course students will be able to:

1. Estimate the complexity of algorithms, understand the general classes of computational problems and graph algorithms.
2. Develop the partition for the given design.
3. Develop and change the floorplans in an abstract manner and use computer algorithms tomake large and optimized floorplans.
4. Create optimized module placement on silicon chips and perform the routing of the modules and clock signal using algorithms.
5. Understand timing analysis and relevant optimizations in placement, routing and netlist restructuring.
6. Understand the use of machine learning in VLSI computer aided design.

Module:1	Introduction	8 hours
VLSI CAD Abstraction Levels, Algorithms and Complexity, Graph Theory Terminology, Graph Traversal/Search- Breadth First Search, Depth First Search, Topological Ordering, Minimum Spanning Tree- Kruskal's Algorithm, Prim's Algorithm, Shortest Paths in Graphs- Dijkstra's Algorithm, Preliminary Taxonomy for Machine Learning in VLSI CAD.		
Module:2	**Circuit Partitioning**	**6 hours**
Problem Formulation, Approaches to Partitioning Problem- Kernighan-Lin Algorithm (Weighted), Fiduccia Mattheyses Heuristic, Simulated Annealing.		
Module:3	**Chip Planning**	**7 hours**
Problem Formulation, Approaches to Floor Planning Problem- Wong-Liu algorithm, Stockmeyer.		
Module:4	**Placement**	**5 hours**
Problem Definition, Cost Functions and Constraints, Approaches to Placement- Min-cut Heuristic, Analytic Placement, Machine Learning for Datapath Placement		
Module:5	**Routing**	**8 hours**
Problem Definition, Cost Functions and Constraints, Maze Routing Algorithms- Lee Algorithm, Power and Ground Routing, Global Routing- Routing Regions, Sequential Global Routing, Channel Routing- Problem Definition, Left-Edge Algorithm, Dogleg Algorithm, Switchbox Routing, Machine Learning for Routability-Driven Placement.		
Module:6	**Specialized Routing**	**5 hours**
Introduction to Area Routing, Net Ordering in Area Routing, Non-Manhattan Routing,		

Basic Concepts in Clock Networks, Modern Clock Tree Synthesis, Machine Learning for Clock Optimization.		
Module:7	**Timing Closure**	**4 hours**
Timing Analysis and Performance Constraints, Timing-Driven Placement, Timing-Driven Routing, Physical Synthesis.		
Module:8	**Contemporary issues:**	**2 hours**
Guest lectures from Industries and R&D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Andrew B. Kahng, VLSI Physical Design: From Graph Partitioning to Timing Closure, 2022, 2nd Edition, Springer.
2.	Sadiq M. Sait and Habib Youssef, VLSI Physical Design Automation: Theory and Practice, 1999, 1st Edition, World Scientific Publishers.
3.	Ibrahim M. Elfadel, Duane S. Boning, and Xin Li, Machine learning in VLSI Computer-Aided Design, 2019, 1st Edition, Springer.
Reference Books	
1.	Sung Kyu Lim, Practical Problems in VLSI Physical Design Automation, 2011, 2nd Edition, Springer.
2	Naveed A. Sherwani, Algorithms for VLSI Physical Design Automation, 2012, 2nd Edition, Springer.
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.	

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD304L	CMOS Analog IC Design	3	0	0	3
Pre-requisite	BEVD204L, BEVD204P	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Understand the relationships between devices and circuits.
2. Analyze and design single-ended and differential IC amplifiers.
3. Understand the feedback configurations.
4. Emphasize the design of practical amplifiers, and their performance parameters tradeoffs.

Course Outcomes

After completion of the course, the student will be able to:

1. Understand the basic MOSFET operation, second order effects, and current sources
2. Design single-stage, differential amplifiers, and analyse the performance with respect to frequency and noise
3. Understand the feedback concepts.
4. Design multistage amplifier.
5. Understand frequency compensation techniques of op-amp and its stability analysis
6. Understand the fundamentals of bandgap references

Module:1	MOSFET Current Mirrors and Reference Circuits	8 hours

Review of MOS Device Physics- MOS Device models, MOS Current Sources and Sinks, Current Mirror- Basic Current Mirrors, Cascode Current Mirrors, BiCMOS Circuits, Bandgap References.

Module:2	Basic MOS amplifiers- frequency response and noise	8 hours

Common Source stage, Common Gate stage, Common Drain stage, Cascode stage, Miller effect, Frequency response of Common Source stage, Common Gate stage, Common Drain stage, Cascode stage, Noise in single stage amplifiers.

Module:3	Differential amplifiers- frequency response and noise	4 hours

Differential stage- Single-ended and Fully Differential operation, Basic Differential Pair- Frequency response of differential amplifier, Noise in differential amplifiers.

Module:4	Feedback Amplifiers	6 hours

Ideal feedback equation, Gain sensitivity, Effect of Negative Feedback on Distortion, Types of Feedback Amplifiers, Feedback configurations- voltage-voltage, current-voltage, current-current, voltage-current feedback.

Module:5	Operational amplifiers	7 hours

Common mode Feedback circuits, op-amp CMRR requirements, Need for Single and Multistage amplifiers, Effect of loading in Differential stage. Performance Analysis- DC gain, Frequency response, Noise, Mismatch, Slew rate of cascode and two-stage op-amps, Fully Differential op-amps, Comparators.

Module:6	Stability and frequency compensation	6 hours

Basic Concepts, Instability and the Nyquist Criterion, Effect of Pole Locations on Stability, Frequency Compensation- Concepts and Techniques for Frequency Compensation- Dominant pole, Miller Compensation, Compensation of Miller RHP Zero, Nested Miller, Compensation of two stage op-amp.		
Module 7	**Phase Locked Loop**	**4 hours**
Basic PLL and its dynamics, Charge-pump PLL, Non-ideal Effects in PLL.		
Module:8	**Contemporary issues**	**2 hours**
Guest lectures from Industries and R&D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2017, 2nd Edition, McGraw-Hill.
2.	David Johns and Ken Martin, Analog Integrated Circuit Design, 2012, 2nd Edition, John Wiley & Sons, Inc.
Reference Books	
1.	Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 2016, 2nd Edition, Oxford University Press.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD304P	CMOS Analog IC Design Lab	0	0	2	1
Pre-requisite	BEVD204L, BEVD204P	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Analyze and design single-ended and differential IC amplifiers.
2. Understand the relationships between devices, and circuits
3. Emphasize the design of practical amplifiers, and their performance parameters trade-offs.
4. Understand noise analysis in single stage amplifiers.

Course Outcomes

At the end of the course the student will be able to:

1. Design and characterize single stage amplifiers, according to design specifications in industry standard EDA tool.
2. Design and characterize differential amplifiers, according to design specifications in industry standard EDA tool.

Indicative Experiments		
1.	Simulation of MOSFET IV Characteristics, Second order parameters.	2 hours
2.	Analysis and Design of Simple Current Mirror and Cascode Current Mirror.	2 hours
3.	Design of Single Stage Amplifiers- Common Source, Common Gate and Common Drain.	6 hours
4.	Analysis and Design of Differential Amplifier with resistive load.	2 hours
5.	Analysis and Design of Differential Amplifier with Active load and Current Source Load.	4 hours
6.	Layout of differential amplifier and post-layout simulation.	6 hours
7.	Analysis and Design of Two-Stage op-amp with Frequency Compensation.	6 hours
8.	Noise analysis of single stage amplifier.	2 hours
	Total Laboratory Hours	**30 hours**

Mode of Evaluation: Mode of Assessment: Continuous Assessment Test and Final Assessment Test

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD305L	VLSI Technology	3	0	0	3
Pre-requisite	BEVD101L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Introduce the fundamentals of VLSI manufacturing processes and technology.
2. Understand the various patterning techniques and their limitations.
3. Have a better understanding of thin film deposition and etching techniques.
4. Have a conceptual knowledge of various metals used in gate and packaging.

Course Outcomes

After the completion of the course, the student will be able to:

1. Understand the physics of the Crystal growth, wafer fabrication, and basic properties of silicon wafers.
2. Learning lithography techniques and concepts of wafer exposure systems, types of resists etc.
3. Understand Concepts of thermal oxidation and Si/SiO_2 interface, defects, and its quality measurements.
4. Learn concepts of thin film deposition including Chemical Vapor Deposition and Physical vapor deposition.
5. Understand the concept of etching.
6. Understand back-end technology to define contacts, interconnect, gates, source and drain, and measurement techniques to ensure the quality of designs.

Module:1	**Introduction to Semiconductor Manufacturing and fabrication**	**5 hours**
Introduction to Semiconductor Manufacturing and fabrication (Si, III-V devices), Clean Room types and standards, Crystal structure, Czochralski growth method, Wafer preparation, and defects.		
Module:2	**Lithography Process**	**7 hours**
The Photolithographic Process, Photomask Fabrication, Comparison between positive and negative Photoresists, Exposure Systems, Characteristics of Exposure Systems, Baking, and development, Mask making, E-beam Lithography, Nano imprint lithography.		
Module:3	**Thermal Oxidation of Silicon**	**6 hours**
The Oxidation Process, Masking Properties of Silicon Dioxide, Technology of Oxidation, Characterization methods, Segregation, Interfacial dopant pileup, oxidation-enhanced diffusion, and dopant-defect interaction.		
Module:4	**Diffusion and Ion Implantation**	**6 hours**
Basic concepts, Diffusion process and models, High energy and ultralow energy implantation, shallow junction formation & modeling, Electronic stopping, Damage production and annealing, RTA Process and dopant activation.		
Module:5	**Introduction to thin film deposition**	**8 hours**
Chemical Vapour Deposition (CVD) and its types (thermal, plasma-enhanced, metal-organic), Thermal and e-beam evaporation, DC sputtering, RF sputtering, Atomic Layer Deposition (ALD), Molecular Beam Epitaxy (MBE), Electrodeposition.		
Module:6	**Etching**	**5 hours**

Wet etching, Plasma etching, RIE, Etching of materials used in VLSI.		
Module:7	**Metallization and packaging**	**6 hours**
Contacts, Vias, Multi-level Interconnects, Silicide gates and S/D regions, Reflow & planarization, Multi-chip modules, packaging and its types.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	R.C. Jaeger, Introduction to microelectronic fabrication, 2nd edition, 2013, Pearson.
2.	J.D. Plummer, M. Deal, P.D. Griffin, Silicon VLSI Technology: Fundamentals, Practice, Modeling, 2009, 2nd edition, Prentice Hall.
Reference Books	
1.	S.A. Campbell, Fabrication Engineering at the Micro- and Nanoscale, 2013, 4th edition, Oxford University Press.
2.	S.K. Ghandhi, VLSI fabrication principles, 2009, 2nd edition, John Wiley & Sons inc.
3.	S.M. Sze, VLSI Technology, 2017, 2nd edition, Tata McGraw-Hill.
4.	Shubham Kumar, Ankaj Gupta, Integrated Circuit Fabrication, 2021,1st edition, C.R.C Press.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD305P	VLSI Technology Lab	0	0	2	1
Pre-requisite	BEVD101L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Provide hands-on exposure to simulation/techniques used for VLSI device manufacturing.

Course Outcomes

After completion of the course, the student will be able to:

1. Gain hands-on experience in IC fabrication techniques and related simulation-based tools.

Indicative Experiments

1.	Silicon wafer dicing, pre-cleaning	2 hours
2.	Pre-cleaning of substrate	2 hours
3.	Oxidation of silicon wafer	4 hours
4.	Thermal Evaporation of metal onto a substrate	4 hours
5.	DC sputtering of metal onto a substrate	2 hours
6.	Optical microscopy characterization of the deposited materials	2 hours
7.	C-V characteristics of fabricated MOSFET/MOS Capacitor	2 hours
8.	Introduction to oxidation modeling	2 hours
9.	SUPREM-based modeling for SiO_2 growth of various processes.	2 hours
10.	Sentaurus process for modeling materials regarding dimensionality	2 hours
11.	Sentaurus process for modeling 2D materials-based transistor	2 hours
12.	Modeling the surface topography of deposited materials and predicting their properties.	4 hours
	Total Laboratory Hours	**30 hours**

Mode of assessment: Continuous Assessment Test and Final Assessment Test

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BECE320E	Embedded C Programming	2	0	2	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

1. To impart logical thinking and fundamental problem-solving skills via the use of a programming language.
2. To develop basic and advanced programming concepts using C and Embedded C language.
3. To interface with microcontroller using Embedded C language.

Course Outcomes

The student will be able to

1. Apply the C programming language for various data types and decision making applications.
2. Comprehend the derived data types, pointers and creation of functions.
3. Describe the architecture of 8051 microcontroller for programming & interfacing applications.
4. Write the embedded C code to 8051 for programming I/O ports, timers, serial communication, interrupt and interfacing external peripherals.
5. Develop microcontroller based applications.

Module:1	Introduction to C	3 hours

Introduction to Embedded C, difference between C and Embedded C. Introduction to C programming, comments, identifiers, variables, headers, data types, operators, order of operations, format specifies, escape sequence characters, input and output statements, programs on sequential statements.

Module:2	Control and loop statements	4 hours

Control statements: if, if-else, if-else ladder, elseif ladder, switch. Loops: do-while, while, for loops and nested loops. Break, continue, goto and exit statements. Programs on if, switch and loops.

Module:3	Arrays and strings	3 hours

Arrays: one dimensional and multi-dimensional array, programs on arrays. Strings, functions, pointers.

Module:4	Introduction to 8051 microcontroller	6 hours

Introduction to microcontroller, difference between microcontroller and microprocessor, 8051 : architecture, pin diagram of 8051, memory organization, special function registers, I/O pins ,timers, interrupts, serial interface, power consumption, external interface of the standard 8051.

Module:5	8051 programming in C	4 hours

Data types: sbit, sfr, and bit. Producing delay using loops, programming I/O ports: bit addressable and byte addressable programming, programs on sending and receiving data through I/O ports. Programs on logic operations, data conversion, data serialization with I/O ports.

Module:6	Timer and serial port programming	4 hours

Programs on accessing timers registers, programs on producing time delay using mode 1 and mode 2, programs on generating various clock frequencies, programming of timers 0 and 1 as counters. Serial port programming: transmitting

and receiving data with different baud rates. Programs on timer and Serial communication interrupts.		
Module:7	**Interfacing with displays and sensors**	**4 hours**
Programming of keyboard interfacing, programming of LEDs interfacing, programming of seven segment display interfacing, interfacing circuit description and programming of 16 x 2 LCD, ADC, DAC and temperature sensor interfacing.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**30 hours**
Text Book(s)		
1	Mike McGrath, C Programming in easy steps, 2019, 4th Edition, In Easy Steps Limited.	
2	Muhammad Ali Mazidi , Janice Gillispie Mazidi , Rolin McKinlay, 2014, The 8051 Microcontrollers & Embedded Systems , 2nd edition, Pearson.	
Reference Books		
1.	Barrett, Michaell, and Ambony Massa. Programming Embedded Systems, with C and GNU Development Tools, 2020, O'Reilly Media.	
2	Herbert Schildt, C: The Complete Reference, 2017, 4th Edition, McGraw Hill Education.	
Mode of evaluation: Internal Assessment (CAT, quizzes, Digital Assignments) & Final Assessment Test (FAT)		
Lab Component :		
Indicative Experiments		
1	Programs on Sequential statements	2 hours
2	Programs on Condition and Control statements	2 hours
3	Programs on Arrays	2 hours
4	Programs on Strings & Functions	2 hours
5	Programs on I/O ports	2 hours
6	Programs on Timer/Counter	4 hours
7	Programs on serial communication	2 hours
8	Programs on Timer Interrupts	2 hours
9	Programs on Serial Communication Interrupts	2 hours
10	Programs on External interrupts	2 hours
11	Programs on interfacing Keypad and LCDs	4 hours
12	Programs on interfacing ADC, DAC and Sensors	4 hours
	Total Laboratory Hours	**30 hours**
Mode of assessment: Continuous assessment and FAT		
Recommended by Board of Studies	07-11-2023	
Approved by Academic Council	No. 72 Date	13-12-2023

Course Code	Course Title	L	T	P	C
BECE320E	Embedded C Programming	2	0	2	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

1. To impart logical thinking and fundamental problem-solving skills via the use of a programming language.
2. To develop basic and advanced programming concepts using C and Embedded C language.
3. To interface with microcontroller using Embedded C language.

Course Outcomes

The student will be able to

1. Apply the C programming language for various data types and decision making applications.
2. Comprehend the derived data types, pointers and creation of functions.
3. Describe the architecture of 8051 microcontroller for programming & interfacing applications.
4. Write the embedded C code to 8051 for programming I/O ports, timers, serial communication, interrupt and interfacing external peripherals.
5. Develop microcontroller based applications.

Module:1	Introduction to C	3 hours

Introduction to Embedded C, difference between C and Embedded C. Introduction to C programming, comments, identifiers, variables, headers, data types, operators, order of operations, format specifies, escape sequence characters, input and output statements, programs on sequential statements.

Module:2	Control and loop statements	4 hours

Control statements: if, if-else, if-else ladder, elseif ladder, switch. Loops: do-while, while, for loops and nested loops. Break, continue, goto and exit statements. Programs on if, switch and loops.

Module:3	Arrays and strings	3 hours

Arrays: one dimensional and multi-dimensional array, programs on arrays. Strings, functions, pointers.

Module:4	Introduction to 8051 microcontroller	6 hours

Introduction to microcontroller, difference between microcontroller and microprocessor, 8051 : architecture, pin diagram of 8051, memory organization, special function registers, I/O pins ,timers, interrupts, serial interface, power consumption, external interface of the standard 8051.

Module:5	8051 programming in C	4 hours

Data types: sbit, sfr, and bit. Producing delay using loops, programming I/O ports: bit addressable and byte addressable programming, programs on sending and receiving data through I/O ports. Programs on logic operations, data conversion, data serialization with I/O ports.

Module:6	Timer and serial port programming	4 hours

Programs on accessing timers registers, programs on producing time delay using mode 1 and mode 2, programs on generating various clock frequencies, programming of timers 0 and 1 as counters. Serial port programming: transmitting

and receiving data with different baud rates. Programs on timer and Serial communication interrupts.		
Module:7	**Interfacing with displays and sensors**	**4 hours**
Programming of keyboard interfacing, programming of LEDs interfacing, programming of seven segment display interfacing, interfacing circuit description and programming of 16 x 2 LCD, ADC, DAC and temperature sensor interfacing.		
Module:8	**Contemporary Issues**	**2 hours**
	Total Lecture hours:	**30 hours**
Text Book(s)		
1	Mike McGrath, C Programming in easy steps, 2019, 4th Edition, In Easy Steps Limited.	
2	Muhammad Ali Mazidi , Janice Gillispie Mazidi , Rolin McKinlay, 2014, The 8051 Microcontrollers & Embedded Systems , 2nd edition, Pearson.	
Reference Books		
1.	Barrett, Michaell, and Ambony Massa. Programming Embedded Systems, with C and GNU Development Tools, 2020, O'Reilly Media.	
2	Herbert Schildt, C: The Complete Reference, 2017, 4th Edition, McGraw Hill Education.	
Mode of evaluation: Internal Assessment (CAT, quizzes, Digital Assignments) & Final Assessment Test (FAT)		
Lab Component :		
Indicative Experiments		
1	Programs on Sequential statements	2 hours
2	Programs on Condition and Control statements	2 hours
3	Programs on Arrays	2 hours
4	Programs on Strings & Functions	2 hours
5	Programs on I/O ports	2 hours
6	Programs on Timer/Counter	4 hours
7	Programs on serial communication	2 hours
8	Programs on Timer Interrupts	2 hours
9	Programs on Serial Communication Interrupts	2 hours
10	Programs on External interrupts	2 hours
11	Programs on interfacing Keypad and LCDs	4 hours
12	Programs on interfacing ADC, DAC and Sensors	4 hours
	Total Laboratory Hours	**30 hours**
Mode of assessment: Continuous assessment and FAT		
Recommended by Board of Studies	07-11-2023	
Approved by Academic Council	No. 72 Date	13-12-2023

BEIE394J	Product Development Project	L	T	P	C
		0	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives:

1. Students will be able to translate a prototype to a useful product.
2. Apply relevant codes and standards during product development.
3. The student will be able to present his results by means of clear technical reports.

Course Outcome:

1. Demonstrate the ability to translate the developed prototype/working model to a viable product useful to society/industry.
2. Apply the appropriate codes/regulations/standards during product development.
3. Write clear and concise technical reports and research articles

Module Content

Students are expected to translate the developed prototypes / working models into a product which has application to society or industry.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered. Assessment on the project – Mark weightage of 20:30:50 – Report to be submitted, presentation and project reviews

Recommended by Board of Studies	09-03-2022		
Approved by Academic Council	No.65	Date	17-03-2022

Course Code	Course Title	L	T	P	C
BEVD208L	2D Materials and Devices	3	0	0	3
Pre-requisite	BEVD101L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Give students an idea about various 2D materials and their applications.
2. Understand in-depth the synthesis and characterization of various 2D materials.
3. Introduce the different modelling and simulation tools associated with 2D materials and devices.
4. Acquire knowledge about various characterization techniques of 2D materials

Course Outcomes

After completing this course, students shall be able to:

1. Identify the 2D materials and understand their band structure.
2. Gain knowledge of the synthesis techniques used for graphene.
3. Understand the various applications of graphene-based devices.
4. Gain knowledge of the synthesis techniques used for non-graphene-based 2D materials.
5. Understand the various applications of MXenes, Phosphorene, etc., and gain familiarity with the modeling tools.
6. Gain knowledge of the characterization techniques of 2D materials.

Module:1	Introduction to 2D materials	4 hours

Introduction to 2D materials, electronic band structure in 2D materials, Types of 2D materials, electronic properties of conventional thin film vs thick nanosheet vs single layer nanosheet.

Module:2	Graphene: Synthesis	7 hours

Mechanical and chemical exfoliation, solution techniques, CVD, thermal decomposition of SiC, unzipping of CNT, graphene oxide (GO) and rGO.

Module:3	Applications of graphene	7 hours

Transistor fabrication, optoelectronics, sensors, spintronics, solar cells, Displays and touch screens.

Module:4	Introduction to MXenes, TMDCs	7 hours

Top-down and bottom-up synthesis methods for 2D transition metal carbides and nitrides, physical and chemical synthesis methods for 2D transitional metal dichalcogenide, properties of phosphorene, silicene, Germanene and stanene

Module:5	MXenes, TMDC-based devices	5 hours

2D Semiconductor FET, Energy storage devices (Batteries, supercapacitors), Optoelectronic devices (LED, LASER), photovoltaic devices, sensors, catalysis

Module:6	Device Modeling of 2D materials	6 hours

Computational modeling of 2D materials, TCAD based device modeling of 2D devices

Module:7	Characterization of 2D materials	7 hours

Raman spectroscopy, HRTEM, optical characterization, AFM, STM, XPS

Module:8	Contemporary Issues	2 hours

Guest lecture from Industries and R & D Organizations

	Total Lecture hours:		**45 hours**
Text Book(s)			
1.	Phaedon Avouris, Tony F. Heinz, Tony Low, 2D Materials: Properties and Devices, 2017, 1st edition, Cambridge University Press, U.K		
2.	Luigi Colombo, Rafik Addou, Defects in Two-Dimensional Materials, 2022, 1st edition, Elsevier Science.		
Reference Books			
1.	Babak Anasori, Yury Gogotsi, 2D Metal Carbides and Nitrides (MXenes) Structure, Properties and Applications, 2019, 1st edition, Springer.		
2.	C N R Rao, Umesh Vasudeo Waghmare, 2D Inorganic Materials Beyond Graphene, 2017,1st edition, World Scientific Publishing Company.		
3.	Ashish Raman, Deep Shekhar, Naveen Kumar, Sub-Micron Semiconductor Devices: Design and Applications, 2022, 1st edition, CRC Press.		
4.	Saptarshi Das, 2D Materials for Electronics, Sensors and Devices: Synthesis, Characterization, Fabrication and Application, 2022, 1st edition, Elsevier Science.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD210L	Quantum Technology for Electronics Engineers	3	0	0	3
Pre-requisite	BPHY101L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Educate the students on concepts of quantum theory and its importance
2. Make the students understand the importance of quantum effects in devices
3. Enable the students to apply quantum theory in the design of nanoscale devices

Course Outcomes

The students will be able to

- Apply the concepts of quantum theory in semiconductor devices
- Understand the importance of Schrodinger wave equation & its applications.
- Obtain the knowledge on quantum confinement effects.
- Gain the knowledge in dispersion relations of electrons in solids.
- Understand the perturbation theory and its applications.
- Understand and apply the concept of quantum computation

Module:1	Elementary Principles and Applications to Problems in one dimensions	5 hours

Waves and particles: Light as particles—the photoelectric, Electrons as waves, Position and momentum, Expectation of the position, Momentum, Non-commuting operators. The Schrodinger equation - Waves and the differential equation, Density and current, The free particle, A potential step, The infinite potential well, The finite potential well, The triangular well, Coupled potential wells, The Ehrenfest theorem.

Module:2	Tunnelling Phenomena in Devices	8 hours

The tunnel barrier: The simple rectangular barrier, The tunnelling probability, A more complex barrier, The double barrier, Simple, equal barriers, The unequal-barrier case, Shape of the resonance, Approximation methods—the WKB method, Bound states of a general potential, Periodic potentials - Velocity, Superlattices Tunnelling, Tunnelling devices, A current formulation, The Landauer formula, The resonant tunnelling diode, Resonant interband tunneling. Single-electron tunneling, The double-barrier quantum dot.

Module:3	The harmonic oscillator	5 hours

Periodic potential, Bloch oscillations, The wavefunction, Motion of the wave packet, A simpler approach with operators, Quantizing the LC Circuit, The vibrating lattice, Motion in a quantizing magnetic field, Connection with classical orbits, Adding lateral confinement.

Module:4	Basis functions, operators, and quantum dynamics	6 hours

Position and momentum representation, operator properties: Time-varying expectations, Hermitian operators, On commutation relations. Linear vector spaces: matrix properties, The eigenvalue problem, Dirac notation. Fundamental quantum

postulates: Translation operators, Discretization and superlattices, Time as a translation operator, Canonical quantization.		
Module:5	**Perturbation Theory**	**6 hours**
Stationary perturbation theory: The perturbation series, Some examples of perturbation theory - The Stark effect in a potential well, The shifted harmonic oscillator, Multiple quantum wells, Coulomb scattering. An alternative technique—the variational method. Time-dependent perturbation theory: The perturbation series, Electron–phonon scattering, The interaction representation, Exponential decay and uncertainty.		
Module:6	**Motion in centrally symmetric potentials**	**7 hours**
The two-dimensional harmonic oscillator: Rectangular coordinates, Polar coordinates, Splitting the angular momentum states with a magnetic field, Spectroscopy of a harmonic oscillator. The hydrogen atom - The radial equation, Angular solutions, Angular momentum, Atomic energy levels, The Fermi–Thomas model, The Hartree self-consistent potential, Corrections to the centrally symmetric potential, The covalent bond in semiconductors.		
Module:7	**An Introduction to Quantum Computing**	**6 hours**
Qubits and Entanglement, Quantum Dots for Qubits, Josephson Junctions, Optical Qubits, Quantum Communication and Cryptography.		
Module:8	**Contemporary issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**
Text Book(s)		
1.	David K Ferry, Quantum Mechanics: An Introduction for Device Physicists and Electrical Engineers, 2020, 3rd Edition, CRC Press.	
2.	A. F. J. Levi, Applied Quantum Mechanics, Second Edition, 2023, 3rd Edition, Cambridge University Press.	
Reference Books		
1.	Jasprit Singh, Quantum Mechanics: Fundamentals and Applications to Technology, 2004, 1st edition, Wiley-VCH.	
2.	Dennis M. Sullivan, Quantum Mechanics for Electrical Engineers, 2012, 1st edition, Wiley & IEEE.	
3.	David A. B. Miller, Quantum Mechanics for Scientists and Engineers, 2008, 1st edition, Cambridge University Press.	
4.	Richard L. Liboff, Introductory Quantum Mechanics, 2003, 4th edition, Pearson Education Inc, India.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.		
Recommended by Board of Studies	05-11-2024	
Approved by Academic Council	No. 76	Date 27-11-2024

Course Code	Course Title	L	T	P	C
BEVD211L	Thin Films Characterization	3	0	0	3
Pre-requisite	BEVD101L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Learn about the wide range of analysis techniques available.
2. Understand the basic principles of the analysis techniques.
3. Gain knowledge of X-ray based thin-film characterization techniques.
4. Acquire knowledge of electrical and mechanical characterization of thin films and advanced characterization techniques

Course Outcomes

After completing this course, students shall be able to:

1. Understand the thickness measurement techniques of thin films
2. Understand the Optical characterization techniques of thin films
3. Understand the electron microscopy-based characterization techniques of thin films
4. Analyzing crystallinity and phase analysis of thin films using X-ray techniques.
5. Understand and analyze the electrical and mechanical property measurements of thin films
6. Know about the advanced thin film characterization techniques

Module:1	Introduction to thin films and thickness measurement techniques	4 hours

Definition of thin films- thin film properties, Thickness measurement: Profilometry- working principle and analysis, spectroscopic ellipsometry, and Quartz Crystal Microbalance (QCM).

Module:2	Optical characterization techniques	6 hours

Introduction to optical microscopy, UV-Vis spectroscopy- working principle and band gap measurements, and Ultraviolet photoelectron spectroscopy (UPS).

Module:3	Electron microscopy and in-situ measurements	8 hours

Scanning electron microscopy –working principle, types of sources (thermionic, field emission), Energy-dispersive X-ray spectroscopy, morphological analysis, Transmission electron microscopy- working principle, types (High resolution-, Aberration corrected, In-situ), Real and reciprocal lattice, Selected Area Electron Diffraction (SAED) technique, Overview of AFM and modes of operation.

Module:4	X-ray-based characterization techniques	8 hours

Fundamentals of X-ray scattering- Bragg's law, types of X-ray sources. X-ray diffraction and its methods, Determination of crystal structure, precise lattice parameter, and phase diagram, Introduction to XPS, XRF.

Module:5	Electrical property measurements	6 hours

Van der pauw method, Hall effect measurement, Probe station (I-V and C-V measurements)

Module:6	Mechanical property measurements	4 hours

Thin film stress measurement, beam bending test, Vickers hardness measurement and nano-indentation, Indirect measurement techniques.

Module:7	Advanced Characterization techniques	7 hours

Reflection High Energy Electron Diffraction (RHEED), Secondary Ion Mass

Spectroscopy (SIMS), and Raman spectroscopy.			
Module:8	**Contemporary Issues**		**2 hours**
Guest lecture from Industries and R & D Organizations			
	Total Lecture hours:		**45 hours**
Text Book(s)			
1.	Milton Ohring, Materials Science of Thin Films: Deposition and Structure, 2002, 2nd edition, Elsevier.		
2.	Terry L. Alford, L.C. Feldman, James W. Mayer, Fundamentals of Nanoscale Film Analysis, 2007, 1st edition, Springer.		
Reference Books			
1.	Hamid R. Khan, Hartmut Frey, Handbook of Thin Film Technology, 2015, 1st edition, Springer.		
2.	B. D. Cullity and S. R. Stock, Elements of x-ray Diffraction, 2001, 3rd edition, Prentice-Hall Publishers.		
3.	R. Egerton, Physical Principles of Electron Microscopy: An Introduction to TEM, SEM, and AEM, 2005, 1st edition, Springer.		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD306L	Photovoltaics and Energy Conversion Devices	3	0	0	3
Pre-requisite	BEVD201L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Gain knowledge on solar energy conversion principles.
2. Learn the fundamentals of semiconductors and their application for solar cell fabrication and characterization.
3. Develop an understanding of solar photovoltaic power systems from the module assembly process.
4. Know the necessary details of the establishment and commissioning of the solar photovoltaic power plant.

Course Outcomes

After completing this course, students shall be able to:

1. Gain knowledge of basic principles related to solar energy and energy conversion devices.
2. Understand the material properties and the techniques involved in solar cell fabrication.
3. Analyze the solar cell devices and able to characterize them.
4. Gain knowledge of emerging solar cell technologies.
5. Understand the assembly of Solar Cell modules.
6. Design the Solar PV System and gain knowledge of advanced SPV Technologies.

Module:1	Solar Energy and Energy conversion device principles	5 hours

Solar radiation: measurements and prediction. India's solar energy potential and challenges, solar energy conversion principles and technologies: Photosynthesis, Photovoltaic conversion, and Photothermal energy conversion.
Need for Renewable energy – sustainability – wind energy – thermal energy – hydro energy – solar energy.

Module:2	Materials and Solar Device fabrication	7 hours

Transparent conducting oxides-Anti-reflection principles and coatings – organic materials Semiconductor junctions: Schottky barriers, MIS, P-N junction, p-i-n junction and its properties, Homo & heterojunction solar cells, multijunction solar cells- Fabrication techniques: Diffusion, thin film technology– Nanotech solar cells- contact & grid metallization.

Module:3	Characterization and Analysis	7 hours

Device isolation & analysis - Ideal cell under illumination- solar cell parameters short circuit current, open circuit voltage, fill factor, efficiency; optical losses; electrical losses, surface recombination velocity, quantum efficiency - measurements of solar cell parameters; I-V curve & L-I-V characteristics, internal Quantum yield measurements – Effects of series and parallel resistance and Temperature - Loss analysis.

Module:4	Emerging solar cell technologies	7 hours

Structures and operation: Copper indium gallium selenide-based solar cells, cadmium telluride solar cells, Organic solar cells, Dye-sensitized solar cells, Perovskite solar cells, Quantum dot solar cells, Polymer solar cells.

Module:5	Solar Cell Module Materials and Assembly	7 hours
PV modules: Module and Circuit Design - Identical and Non-identical Cells - Module Structuring and assembly - Environmental Protection - Thermal Considerations - Electrical Considerations and output conditioning - assembly materials – interconnects – crystalline and thin film modules - issues with solar PV modules, bypass diode and blocking diode – module testing and analysis.		
Module:6	**Solar PV System Components & System Design**	**6 hours**
Introduction to PV systems - system components: module and array – Charge controllers – inverters – Batteries – power conditioning and Regulation – Mechanical assemblies – Balance of System Components MW general power systems – Grid-connected power systems – Remote area power systems – Specific purpose Photovoltaic systems: Space – Marine – Telecommunication – water pumping – refrigeration etc.		
Module:7	**Advanced SPV Technologies**	**4 hours**
Solar PV concentrators – Concentrator photovoltaic materials and devices – Hybrid SPV power systems – SPV power plant design tools and methodologies – SPV economics.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	Klaus Jäger, Olindo Isabella, Arno H.M. Smets, René A.C.M.M. van Swaaij, Miro Zeman, Solar Energy: Fundamentals, Technology, and Systems, 2016, 1st edition, UIT Cambridge, Cambridge.
2.	Mariana Amorim Fraga, Delaina A. Amos, Savas Sönmezoglu, Velumani Subramaniam, Sustainable Material Solutions for Solar Energy Technologies: Processing Techniques and Applications, 2021, 1st edition, Elsevier.
3.	Gopal Nath Tiwari, Swapnil Dubey, Fundamentals of photovoltaic modules and their applications, 2009, 1st edition, Royal Society of Chemistry.
4.	James P. Dunlop, Photovoltaic Systems, 2010, 2nd Edition, American Technical Publishers.

Reference Books

1.	Michael Boxwell, The Solar Electricity Handbook, 2021, Greenstream Publishing Ltd.
2.	J. Nelson, The physics of solar cells, 2006, 1st edition, Imperial College Press.
3.	Alan L Fahrenbruch and Richard H Bubeg, Fundamentals of Solar Cells: PV Solar Energy Conversion, 2012, 1st edition, Academic Press.
4.	Solar Energy International, Photovoltaics: Design and Installation Manual, 2006, 4th edition, New Society Publishers.
5.	Ben G. Streetman, Solid State electronic devices, 2017, 7th edition, Prentice-Hall of India Pvt. Ltd.
6.	M. D. Archer, R. Hill, Clean electricity from photovoltaics, 2001, 1st edition, Imperial College Press.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD307L	Memory Devices and Circuits	3	0	0	3
Pre-requisite	BEVD201L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Learn the basics and detailed architecture of SRAMs, DRAMs, ROMs, and Flash Memories.
2. Model the memory fault and introduce the basic and advanced memory testing patterns.
3. Elaborate the reliability and radiation effect issues of semiconductor memories and present methods for radiation hardening.
4. Review and discuss high performance memory subsystems, emerging memory technologies and contemporary issues.

Course Outcomes

After completion of the course, the student will be able to:

1. Design SRAMs and DRAMs.
2. Design NVRAMs and Flash Memories.
3. Model memory faults, select suitable testing patterns and develop testing patterns.
4. Incorporate DFT and BIST techniques for semiconductor memory testing.
5. Estimate the reliability of semiconductor memories, simulate and model radiation effects and, perform radiation hardening.
6. Contribute to the development of high performance memory subsystems and use emerging memory technologies.

Module:1	Volatile memories	7 hours

SRAM – SRAM Cell structures, MOS SRAM Architecture, MOS SRAM cell and peripheral circuit operation, SOI technology, Advanced SRAM architectures and technologies, soft error failure in SRAM, CAM, DRAM – DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture

Module:2	Non-volatile memories	8 hours

Masked ROMs, High density ROM, PROM, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture, Ferroelectric Random Access Memories (FeRAMs), Phase Change Memory, Basic Magneto-resistive Random Access Memories (MRAMs) and STT-MRAM-Memory Array Design- Peripheral circuits, Sense amplifier design, NVSim simulator

Module:3	Memory Testing and Patterns	7 hours

General Fault Modeling – Read Disturb Fault Model – Precharge Faults – False Write Through Data Retention Faults – Decoder Faults. Megabit DRAM Testing Nonvolatile Memory Modeling and Testing-IDDQ Fault Modeling and Testing

Application Specific Memory Testing – Zero/one Pattern – Exhaustive Test Patterns – Walking, Matching and Galloping – Pseudo Random Pattern – CAM pattern.		
Module:4	**Design For Test and BIST**	**3 hours**
RAM Built-In Self – Test (BIST)-Weak Write Test mode – Bit Line Contact Resistance – PFET Test – Shadow Write and Shadow Read. BISR. BIRA.		
Module:5	**Reliability and Radiation Effects**	**6 hours**
General Reliability Issues-RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Design for Reliability Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques Radiation Hardening Process and Design Issues-Radiation Hardened Memory Characteristics		
Module:6	**High-Performance Subsystem Memories**	**6 hours**
Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories		
Module:7	**Advanced Memory Technologies**	**6 hours**
High-Density Memory Packaging Technologies, Experimental Memory Devices, RRAM, Memory Hybrids and MCMs (2D)- Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability		
Module:8	**Contemporary issues:**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Shimeng Yu, Semiconductor Memory Devices and Circuits, 2022, 1st edition CRC Press.
2.	R. Dean Adams, High Performance Memory Testing: Design Principles, Fault Modeling and Self-Test, 2013, 1st edition, Springer.
Reference Books	
1.	Baker Mohammed, Embedded Memory Design for Multi-Core and Systems on Chip, 2016, 1st edition, Springer.
2.	Hai Li and Yiran Chen, Nonvolatile Memory Design: Magnetic, Resistive, and Phase Change, 2017, 1st edition, CRC Press.
3.	Kiyoo Itoh, VLSI Memory Chip Design, 2010, 1st edition, Springer.
4.	Hao Yu and Yuhao Wang, Design Exploration of Emerging Nano-scale Non-volatile Memory, 2016, 1st edition, Springer.
5.	Yuan Xie, Emerging Memory Technologies: Design, Architecture, and Applications, 2016, 1st edition, Springer.
6.	A. K.Sharma, Advanced Semiconductor Memories: Architecture, Design and Applications, 2014, 1st edition, John Wiley.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD308L	Low Power VLSI Design	3	0	0	3
Pre-requisite	BECE303L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Introducing the necessity of low power design in VLSI circuits.
2. Provide a broad insight into the methods used to confront the low power issue from lower level (circuit level) to higher levels (system level) of abstraction.
3. Design various low power VLSI circuits.
4. Provide an insight to the power aware IC design

Course Outcomes

After completion of the course the student will be able to:

1. Analyze the need for low power VLSI circuits.
2. Estimate the power consumed in the circuits.
3. Optimize the power at architectural level.
4. Optimize the power at RTL, logic and circuit levels.
5. Analyze and explore the usage of sleep transistors and power gating technique for low power.
6. Explore low power design with UPF inclusion.

Module:1	Introduction to Low Power Design Methods	7 hours

Motivation, Sources of Power dissipation in Deep Submicron CMOS and FINFET Circuits – Static, Dynamic and Short circuit components, Effects of scaling on power consumption, Low power design flow, Normalized Figure of Merit – PDP & EDP, Overview of power optimization at various levels.

Module:2	Power Estimation	5 hours

Theoretical background, Calculation of Steady state probability- Algorithm for signal probability propagation- Shannon's decomposition- BDD, Transition probability, Conditional probability, Transition probability of correlated inputs, Transition density, Estimation of Switching activity.

Module:3	Architecture Level Optimization	8 hours

Pipelining, Parallel Processing and retiming approaches for power minimization, Multiple supply voltage design -challenges - Level shifters- High to Low Voltage, Low to High Voltage- locating level shifters in multiple voltage domains.

Module:4	Register Transfer Level Optimization	4 hours

Clock gating, Data gating, Bus Encoding techniques, Precomputation, Operator reduction and operator substitution for low power.

Module:5	Gate Level and Circuit Level Optimization	6 hours

Transistor variable re-ordering for power reduction, Gate resizing, Low power library cell design (GDI), Optimal drivers of high-speed low power ICs, Approximate computing for reducing power consumption in Adders and Multipliers, Synthesis of FSM for low power.

Module:6	Leakage Power Reduction	7 hours
Leakage power reduction techniques for CMOS and FINFET based circuits, Sleep Transistors, Power gating – coarse grain and fine grain, Switch fabric, Isolation, retention, power down and wake up methods.		
Module:7	**Power Aware Design Flow**	**6 hours**
Power aware design flow, Unified power format (UPF)- Necessity, Power intent for MSV and PSO, UPF for multi supply voltage design examples.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**

Text Book(s)	
1.	Kaushik Roy, Sharat Prasad, Low Power CMOS VLSI Circuit Design, 2010, 2nd edition, John Wiley and Sons Inc.
2.	Ajit Pal, Low Power VLSI circuits and Systems, 2015, 1st edition, Springer India.
Reference Books	
1.	Gary K. Yeap, Practical Low Power Digital VLSI Design, 2010, 1st edition, Springer US,
2.	Jan M. Rabaey, Massoud Pedram, Low power Design Methodologies, 2014, 1st edition, Springer US.
3.	Dimitrios Soudris, Christrian Pignet, Costas Goutis, Designing CMOS circuits for low Power, 2011, 1st edition, Springer US.
4.	Keshab K.Parhi, VLSI Digital Signal Processing Systems: Design and Implementation, 1999, 1st edition, Wiley-Inter Science.
5.	Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, Kaijian Shi, Low power methodology manual: for system-on-chip design, 2008, 2nd Edition, Springer Science & Business Media.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD309L	Testing of VLSI Circuits	3	0	0	3
Pre-requisite	BECE102L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

- Understand the process of testing and its importance in the VLSI design flow.
- Learn the fundamentals of VLSI testing such as fault models, fault simulation, test generation etc.
- Introduce the concept of modeling and simulation of logic and memory testing.
- Familiarize different designs for testability techniques for improving the yield of IC design.

Course Outcomes

After completion of the course, the student will be able to:

- Comprehend different fault models and fault simulation techniques.
- Use suitable ATPG methods for testing VLSI circuits.
- Apply scan based DFT and Boundary scan to improve testability.
- Apply BIST to improve testability.
- Effectively use test vector compression and test response compaction techniques to reduce test time and memory storage.
- Comprehend different memory fault models and test algorithms

Module:1	Need and RTL Required for Testing	7 hours

Importance of Testing - Testing during the VLSI Lifecycle -Challenges in the VLSI Testing, Design Verification, Yield and Reject Rate, Test Generation, Fault Models, Stuck-At Faults, Transistor Faults, Open and Short Faults, Delay Faults and Crosstalk ,Pattern Sensitivity and Coupling Faults, Analog Fault Models Levels of Abstraction in VLSI Testing

Module:2	Fault Modeling and Fault Simulation	7 hours

Fault Abstraction, Functional Faults, Structural Faults, Structural Gate Level Faults, Issues Related to Gate Level Faults, Fault Collapsing - Fault dropping. Fault Simulation Applications - Fault Coverage - Fault Simulation in Test Generation - Fault Dictionary Creation. Fault Simulation Technologies – Serial, Parallel, and deductive Fault Simulation, PDF Vs TDF

Module:3	Test Pattern Generation Methods and Algorithms	7 hours

Test Generation, Test Generation Process, Fault and Tests. Testability Analysis-SCOAP Controllability and Observability for combinational circuits. Random Test Generation - Combinational Circuit Deterministic Test Generation Algorithms - D-Algorithm, Fault-Independent Test Generation

Module:4	Design for Test by Means of Scan	6 hours

Making Circuits Testable, Testability Insertion, Full Scan DFT Technique, Scan Architectures, RT Level Scan Design. RTL Scan Design Rule Checking and Repair - RTL Scan Synthesis- RTL Scan Extraction and Scan Verification, Scan Design Rules- Fixing the DRC Violations and recommended solutions BIST Basics, Test

Pattern Generation - Exhaustive Testing, Pseudo-Random Testing, Pseudo-Exhaustive Testing. Output Response Analysis (ORA), BIST Architectures, RT Level BIST Design		
Module:5	**Logic Built-in Self-test (L-BIST)**	**5 hours**
Boundary Scan Basics, Boundary Scan Architecture, Boundary Scan Test Instructions, Board Level Scan Chain Structure, Introduction to IEEE 1687-IJTAG		
Module:6	**Test Compression**	**6 hours**
Test stimulus Compression - Compression Methods, Scan-based Schemes. Decompression Methods - Test Response Compaction - Space Compaction, Time Compaction		
Module:7	**Memory Testing by Means of Memory BIST**	**5 hours**
Memory Testing, Memory Structure, Memory Fault Model, Functional Test Procedures, March Test Algorithms, March C- Algorithm, MATS+ Algorithm, Other March Tests. BIST with Diagnostic Support, RAM Defect Diagnosis and Failure Analysis, Built-In Self-Repair		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**

Text Book(s)	
1.	Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, VLSI Test Principles and Architectures: Design for Testability, 2006, 1st Edition, Morgan Kaufmann Publishers, USA.
2.	M. Bushnell and Vishwani Agrawal, Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits, Illustrated Edition, 2004, Springer, New York, USA
Reference Books	
1.	Zainalabedin Navabi, Digital System Test and Testable Design: Using HDL Models and Architectures, 2011, 1st Edition, Springer, New York, USA.
2.	Sebastian Huhn and Rolf Drechsler, Design for Testability, Debug and Reliability Next Generation Measures using Formal Techniques, 2021, 1st Edition, Springer, Cham, USA.
3.	Santanu Chattopadhyay, Thermal-Aware Testing of Digital VLSI Circuits and Systems, 2020, 1st Edition, CRC Press, USA.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD311L	VLSI Digital Signal Processing Systems	3	0	0	3
Pre-requisite	BEVD203L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Comprehensive coverage of requirements, representation, and implementation aspects of DSP systems.
2. Detailed understanding and application of architectural optimizations and transformations of DSP algorithms.
3. Implement DSP algorithms in hardware, including finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and other common DSP functions.
4. Effects of pipelining, parallel processing, and finite word length effects of a DSP architecture.

Course Outcomes

After completion of the course, the student will be able to:

- Understand the design requirements and representation of DSP algorithms.
- Calculate iteration bound and analyze the effects of pipelining and parallel processing.
- Understand and apply retiming techniques on a given DSP architecture.
- Understand and apply unfolding techniques on a given DSP architecture.
- Understand and apply folding techniques on a given DSP architecture.
- Analyze a DSP architecture's finite word length effects and scaling.

Module:1	Review of Digital Signal Processing Algorithms	5 hours

Typical DSP Algorithms – DSP Application Demands and Scaled CMOS Technologies – Representations of DSP Algorithms.

Module:2	Iteration Bound	6 hours

Data-Flow Graph Representations – Loop Bound and Iteration Bound – Algorithms for Computing Iteration Bound – Longest Path Matrix and Multiple Cycle Mean algorithms – Iteration Bound of Multi-rate Data Flow Graphs.

Module:3	Pipelining and Parallel Processing	6 hours

Pipelining of FIR Digital Filters – Parallel Processing – Pipelining and Parallel Processing for Low Power – Combined Pipelining and Parallel Processing.

Module:4	Retiming	7 hours

Definitions and Properties of Retiming – Solving Systems of Inequalities – The Bellman-Ford Algorithm – Retiming Techniques: Cutset Retiming and Pipelining.

Module:5	Unfolding	7 hours

An Algorithm for Unfolding – Properties of Unfolding – Critical Path – Unfolding and Retiming – Applications of Unfolding.

Module:6	Folding	6 hours
Introduction – Folding Transformation, Register Minimization Techniques – Register Minimization in Folded Architectures – Folding for Multirate Systems.		
Module:7	**Scaling and Rounding Noise**	**6 hours**
Scaling and Rounding Noise – State Variable Description of Digital Filters, Scaling and Rounding Noise Computation – Rounding Noise in Pipelined IIR Filters – Roundoff Noise Computation using State Variable Description.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**

Text Book(s)	
1.	Parhi, Keshab, VLSI digital signal processing systems: design and implementation, 2007, 1st edition, Wiley India Pvt. Ltd.
2.	Shoab Ahmed Khan, Digital Design of Signal Processing Systems: A Practical Approach, 2011, 1st edition, Wiley India Pvt. Ltd.
Reference Books	
1.	Li Tan, Jean Jiang, Digital Signal Processing: Fundamentals and Applications, 2018, 3rd edition, Cambridge University Press
2.	John G. Proakis, Dimitris G. Manolakis, Digital Signal Processing, 2018, 4th edition, Pearson, United Kingdom.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD313L	Computational Techniques	2	1	0	3
Pre-requisite	BEVD206L, BEVD206P	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Enable students to understand the principles of semiconductor transport as applied to understanding device operation from a physical standpoint.
2. Understand how advanced scientific modeling and simulation can pave the way for semiconductor device optimization and discovery
3. Understand the essential physical processes governing the operation of current state-of-the-art semiconductor devices.
4. Enable students to develop simulation software for modeling arbitrary device structures.

Course Outcomes

After completion of the course, the student will be able to:

- Apply various essential numerical methods in semiconductor device simulation.
- Apply semiclassical and quantum transport models to simulate various charge transport conditions.
- Understand electrostatic conditions for different types of device structures.
- Extract bandgap and effective masses from band structures.
- Analyze various scattering processes and mobility models
- Estimate the semiconductor device's thermal conductivity and optical parameters

Module:1	Introduction and Essential Numerical Methods	7 hours

The importance of computational techniques; different classes of semiconductor devices; and understanding the meaning of device theory-modeling-simulation (TMS) approaches to problem-solving and decision-making; Numerical methods: Finding roots, integration, and differentiation; Solving differential equations: Discretization into a matrix equation, solving matrices, eigenvalues, and eigenvectors.

Module:2	Fundamentals Of Carrier Transport Models	5 hours

Drude's model, Landauer's model, ballistic transport, Wave equations
Quantum transport equations, Boltzmann Transport Equation, Drift-Diffusion model
Hydrodynamic model and Ballistic model.

Module:3	Modeling Electrostatics And Solving Continuity Equations	8 hours

Poisson's equation, Analytical solution, Numerical solution: Discretization, Boundary conditions, Matrix inversion; Solving continuity equations: Numerical solutions of the electron-hole continuity equations. Working assignment on DD transport in PN junction Diode, and MOSFET using MATLAB/TCAD.

Module:4	Electronic Bandstructure Calculation	8 hours

Numerical solution of Schrödinger equation, Wave packet dynamics, Periodic potential, and the Kronig-Penny model; Bandstructure calculation using the tight-binding method: Theory, implementation, case study on a silicon and graphene lattice, Electron density of states, and effective mass.		
Module:5	**Modeling Scattering Processes And Carrier Mobility**	**5 hours**
Phonon modes, Perturbation theory, Scattering rate calculation, RTA, and Rhode's iterative method for mobility modeling and Various mobility models		
Module:6	**Thermoelectrics**	**5 hours**
Thermal conductivity, Self-heating in semiconductor devices, and ZT figure-of-merit of thermoelectric devices.		
Module:7	**Fundamentals Of Optical Processes:**	**5 hours**
Optical transition rate, Internal and external quantum efficiency, Efficiency droop, and lumen depreciation.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**
Text Book(s)		
1.	Dragica Vasileska, Stephen M. Goodnick, and Gerhard Klimeck, Computational Electronics: Semiclassical and Quantum Device Modeling and Simulation, 2010, 1st edition, CRC Press.	
Reference Books		
1.	Mark Lundstorm, Jing Guo, Nanoscale Transistors: Device Physics, Modeling and Simulation, 2005, 1st edition, Springer.	
2.	Mark Lundstorm, Fundamentals of Carrier Transport 2009, 2nd edition, Cambridge University Press.	
3.	John E. Savage, Models of Computation: Exploring the Power of Computing, Addison-Wesley, 2023, online edition, Brown University.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.		
Recommended by Board of Studies	05-11-2024	
Approved by Academic Council	No. 76	Date 27-11-2024

Course Code	Course Title	L	T	P	C
BEVD314L	Mixed Signal Circuit Design	3	0	0	3
Pre-requisite	BEVD204L, BEVD204P	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Introduce the design aspects of dynamic analog circuits and analog-digital interface electronics in CMOS technology.
2. Understanding switched capacitor circuits.
3. Understanding the Nyquist rate ADC & DAC architectures.
4. Familiarization of oversampling converters.

Course Outcomes

After completion of the course, the student will be able to:

1. Design Sample and Hold Circuits using MOSFETs and OP-AMP.
2. Design and Analyze Comparator Circuits
3. Design and Analyze Switched Capacitor Circuits.
4. Understand basics of Data Converters.
5. Understand about Nyquist-rate D/A converters, Nyquist-rate A/D converters and Oversampling converters.
6. Design and implement data converters.

Module:1	Sample-and-hold circuits	5 hours

Introduction– Performance of Sample-and-Hold Circuits, Testing Sample and Holds, MOS Sample-and-Hold Basics, Examples of CMOS S/H Circuits.

Module:2	Introduction to Comparators	5 hours

Comparator Specifications, Using an Opamp for a Comparator, Charge-Injection Errors, Latched Comparators, Examples of CMOS and BiCMOS Comparators.

Module:3	Switched-capacitor circuits	6 hours

Basic Building Blocks, Basic Operation and Analysis, Noise in Switched-Capacitor Circuits, First-Order Filters, Biquad Filters, Charge Injection, Switched-Capacitor Gain Circuits.

Module:4	Data converter metrics	5 hours

Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Signed Codes, Performance Limitations, Resolution, Offset and Gain Error, Accuracy and Linearity.

Module:5	A/D converters	7 hours

Flash Converters, Two-Step A/D Converters, Time-Interleaved A/D Converters, Successive-Approximation Converters, Pipelined A/D Converters.

Module:6	D/A converters	7 hours

Resistor String DAC, R - 2R DAC, Current Steering DAC, Charge Scaling DAC, Pipelined DAC.

Module:7	Oversampling converters	8 hours

Oversampling without Noise Shaping, Oversampling with Noise Shaping, System

Architectures, Digital Decimation Filters, Higher-Order Modulators, Bandpass Oversampling Converters, Practical Considerations.		
Module:8	**Contemporary issues**	**2 hours**
Guest lectures from Industries and R&D Organizations.		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	David Johns and Ken Martin, Analog Integrated Circuit Design, 2012, 2nd edition John Wiley & Sons Inc.
2.	R. Jacob Baker CMOS Circuit Design, Layout, and Simulation, 2019, 4th edition, Wiley-IEEE Press.
Reference Books	
1.	Ahmed M.A. Ali, High Speed Data Converters, 2016, 1st edition, IET Materials, Circuits & Devices.
2.	S.Pavan, R. Schreier and Gabor.C.Temes, Understanding Delta – Sigma Data Converters, 2017, 1st edition, IEEE Press.
3.	R. Jacob Baker Mixed-Signal Circuit Design, 2008, 2nd edition, Wiley-IEEE Press.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD315L	CMOS RF IC Design	3	0	0	3
Pre-requisite	BEVD304L, BEVD304P	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Familiarize with the basic design parameters in radio frequency integrated circuits.
2. Understand the design of transceivers.
3. Familiarize the design of integrated radio frequency front-end circuits
4. Familiarize basic PLL architecture and frequency synthesizer.

Course Outcomes

After completion of the course, the student will be able to:

1. Understand the concepts of RFIC Design.
2. Understand RF transceiver architectures.
3. Analyze Low Noise amplifiers.
4. Analyze Mixers for transceivers.
5. Understand power amplifier topologies.
6. Understand VCOs and PLL architecture.

Module:1	Basic Concepts in RFIC Design	6 hours

MOSFET behavior at RF frequencies- Nonlinearity- Harmonic Distortion Compression, Intermodulation, Noise- Device noise, noise in circuits, Impedance Transformation- Scattering parameters, Matching networks, Passive impedance transformation.

Module:2	Transceiver Architectures	6 hours

Transmitter architectures- Direct-Conversion Transmitters, Heterodyne Transmitters, Receiver Architecture- Basic Heterodyne Receivers, Direct-Conversion Receivers.

Module:3	Low Noise Amplifiers	8 hours

LNA performance parameters, Low Noise Amplifier Topologies- Common Source LNA - Common Gate LNA - Cascode LNA.

Module:4	Mixers	8 hours

Mixer Design parameters, Single balanced and double balanced mixer, Passive down-conversion Mixers, Active down-conversion mixers-Current steering mixer.

Module:5	RF Power Amplifiers	5 hours

General considerations, Class D, Class E, Class F power amplifiers.

Module:6	Phase Locked Loop	5 hours

Building blocks of PLL, Type-I and Type-II PLL Architectures, Noise in PLL, Applications of PLL.

Module:7	VCO and Frequency Synthesizer	5 hours

Basic principle- Cross coupled Oscillator, LC VCOs with wide tuning range, VCO phase noise, Integer-N frequency synthesizer, fractional-N frequency synthesizer.

Module:8	Contemporary issues	2 hours
Guest lectures from Industries and R&D Organizations.		
	Total Lecture hours:	45 hours

Text Book(s)	
1.	Behzad Razavi, RF Microelectronics, 2012, 2nd edition, Prentice Hall.
2.	Thomas H. Lee, The design of CMOS Radio-Frequency Integrated Circuits, 2006, 2nd edition, Cambridge University press.
Reference Books	
1.	Hooman Darabi Radio Frequency Integrated Circuits and Systems, 2020, 2nd edition, Cambridge University Press.
2.	Bosco Leung, VLSI for Wireless Communication, 2011, 2nd edition, Springer.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD391J	Technical Answers to Real Problems Project	0	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives:

1. To gain an understanding of real-life issues faced by society.
2. To study appropriate technologies in order to find a solution to real life issues.
3. Students will design system components intended to solve a real-life issue.

Course Outcomes:

1. Identify real life issue(s) faced by society.
2. Apply appropriate technologies to suggest a solution to the identified issue(s).
3. Design the related system components/processes intended to provide a solution to the identified issue(s).

Module Content	(Project Duration: One Semester)

1. Students are expected to perform a survey and interact with society to find out the real life issues.
2. Logical steps with the application of appropriate technologies should be suggested to solve the identified issues.
3. Subsequently the student should design the related system components or processes which is intended to provide the solution to the identified real-life issues.

General Guidelines:

1. Identification of real-life problems
2. Field visits can be arranged by the faculty concerned
3. Maximum of 3 students can form a team (within the same/different discipline)
4. Minimum of eight hours on self-managed team activity
5. Appropriate scientific methodologies to be utilized to solve the identified issue
6. Solution should be in the form of fabrication/coding/modelling/product design/process design/relevant scientific methodology(ies)
7. Consolidated report to be submitted for assessment
8. Participation, involvement and contribution in group discussions during the contact hours will be used as the modalities for the continuous assessment of the theory component
9. Project outcome to be evaluated in terms of technical, economical, social, environmental, political and demographic feasibility
10. Contribution of each group member to be assessed

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered.
Assessment on the project – Mark weightage of 20:30:50
– Report to be submitted, presentation and project reviews

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD392J	Design Project	0	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives:

1. Students will be able to upgrade a prototype to a design prototype.
2. Describe and demonstrate the techniques and skills necessary for the project.
3. Acquire knowledge and better understanding of design systems.

Course Outcomes:

1. Develop new skills and demonstrate the ability to upgrade a prototype to a design prototype or working model.
2. Utilize the techniques, skills, and modern tools necessary for the project.
3. Synthesize knowledge and use insight and creativity to better understand and improve design systems.

Module Content:	(Project Duration: One Semester)

Students are expected to develop new skills and demonstrate the ability to develop prototypes to design prototype or working models related to an engineering product or a process.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered.
Assessment on the project – Mark weightage of 20:30:50
– Report to be submitted, presentation and project reviews.

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD393J	Laboratory Project	0	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives:

1. The student will be able to conduct experiments on the concepts already learnt.
2. Analyse experimental data.
3. Present the results with appropriate interpretation.

Course Outcomes:

1. Design and conduct experiments in order to gain hands-on experience on the concepts already studied.
2. Analyse and interpret experimental data.
3. Write clear and concise technical reports and research articles.

Module Content	(Project Duration: One Semester)

Students are expected to perform experiments and gain hands-on experience on the theory courses they have already studied or registered in the ongoing semester. The theory course registered is not expected to have laboratory component and the student is expected to register with the same faculty who handled the theory course. This is mostly applicable to the elective courses. The nature of the laboratory experiments is depended on the course.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered.
Assessment on the project – Mark weightage of 20:30:50
– Report to be submitted, presentation and project reviews.

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD394J	Product Development Project	0	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives:

1. Students will be able to translate a prototype to a useful product.
2. Apply relevant codes and standards during product development.
3. The student will be able to present his results by means of clear technical reports.

Course Outcomes:

1. Demonstrate the ability to translate the developed prototype/working model to a viable product useful to society/industry.
2. Apply the appropriate codes/regulations/standards during product development.
3. Write clear and concise technical reports and research articles

Module Content: **(Project Duration: One Semester)**

Students are expected to translate the developed prototypes / working models into a product which has application to society or industry.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered.
Assessment on the project – Mark weightage of 20:30:50
– Report to be submitted, presentation and project reviews

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD396J	Reading Course	0	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives:

1. The student will be able to analyse and interpret published literature for information pertaining to niche areas.
2. Scrutinize technical literature and arrive at conclusions.
3. Use insight and creativity for a better understanding of the domain of interest.

Course Outcomes:

1. Retrieve, analyse, and interpret published literature/books providing information related to niche areas/focused domains.
2. Examine technical literature, resolve ambiguity, and develop conclusions.
3. Synthesize knowledge and use insight and creativity to better understand the domain of interest.

Module Content:	(Project Duration: One Semester)

This is oriented towards reading published literature or books related to niche areas or focussed domains under the guidance of a faculty.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered.
Assessment on the project – Mark weightage of 20:30:50
– Report to be submitted, presentation and project reviews.

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD397J	Special Project	0	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives:

1. Students will be able to identify and solve problems in a time-bound manner.
2. Describe major approaches and findings in the area of interest.
3. Present the results in a clear and concise manner.

Course Outcomes:

1. To identify, formulate, and solve problems using appropriate information and approaches in a time-bound manner.
2. To demonstrate an understanding of major approaches, concepts, and current research findings in the area of interest.
3. Write clear and concise research articles for publication in conference proceedings/peer-reviewed journals.

Module Content: **(Project Duration: One Semester)**

This is an open-ended course in which the student is expected to work on a time bound research project under the supervision of a faculty. The result may be a tangible output in terms of publication of research articles in a conference proceeding or in a peer-reviewed Scopus indexed journal.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered.
Assessment on the project – Mark weightage of 20:30:50
– Project report to be submitted, presentation and project reviews.

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD398J	Simulation Project	0	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives:

1. Students will be able to simulate a real system.
2. Identify the variables which affect the system.
3. Describe the performance of a real system.

Course Outcomes:

1. Demonstrate the ability to simulate and critically analyse the working of a real system.
2. Identify and study the different variables which affect the system elaborately.
3. Evaluate the impact and performance of the real system.

Module Content: **(Project Duration: One Semester)**

The student is expected to simulate and critically analyse the working of a real system. Role of different variables which affect the system has to be studied extensively such that the impact of each step in the process is understood, thereby the performance of each step of the engineering process is evaluated.

Mode of Evaluation: Evaluation involves periodic reviews by the faculty with whom the student has registered.
Assessment on the project – Mark weightage of 20:30:50
– project report to be submitted, presentation and project reviews.

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD402L	AI and Machine Learning for IC	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

This course is aimed at:

1. Understand the importance of Machine learning in IC design.
2. Explore the application of ML techniques in the development of compact lithographic process models and effective mask synthesis for semiconductor manufacturing.
3. Understand and examine the role of ML in physical verification, mask synthesis, and physical design, focusing on optimization and enhancement of VLSI CAD tools.
4. Analyze the performance and efficiency of various AI and ML approaches in the context of IC design.

Course Outcomes

After completion of the course, the student will be able to:

1. Apply the concepts of AI and ML in the context of VLSI CAD to solve real-world engineering problems in IC design.
2. Develop and implement compact lithographic process models using machine learning techniques.
3. Apply ML methods for physical verification and synthesis of VLSI designs, improving design accuracy and performance.
4. Design and evaluate VLSI chip testing protocols incorporating machine learning for enhanced defect detection and process monitoring.
5. Employ machine learning techniques for system optimization and perform uncertainty quantification for integrated systems.
6. Design energy-efficient machine learning hardware, understanding the trade-offs between performance and power consumption in advanced VLSI applications.

Module:1	Introduction to AI and ML in VLSI CAD	8 hours

Review of IC design flow, Artificial Intelligence Techniques and its applications, Level of models, Criteria of success, Intelligent Agents, Nature of Agents, Learning Agents. AI Techniques, Advantages and Limitations of AI, Impact and Examples of AI, Application domains of AI. Machine Learning Taxonomy- Unsupervised, Supervised, and Semi supervised Learning- Discriminative Versus Generative Methods- VLSI CAD Abstraction Levels.

Module:2	Machine learning for compact Lithographic Process Model and Mask Synthesis	8 hours

Introduction-The Lithographic Patterning Process- Machine Learning of Compact Process Models- Neural Network Compact Patterning Models- Machine Learning-Guided optical proximity correction (OPC)- Machine Learning-Guided Etch proximity correction (EPC).

Module:3	Machine Learning in Physical Verification, Mask Synthesis, and Physical Design	5 hours

Machine Learning in Physical Verification- Layout Feature Extraction and Encoding, Machine Learning Models for Hotspot Detection- Machine Learning in Mask Synthesis, Mask Synthesis Flow, Machine Learning for Sub-resolution Assist

Features, Machine Learning for Optical Proximity Correction- Machine Learning in Physical Design		
Module:4	**VLSI Chip Testing and Semiconductor Manufacturing Process Monitoring and Improvement**	**6 hours**
Introduction to VLSI Chip Testing and Semiconductor Manufacturing Process Monitoring and Improvement- Machine Learning for Chip Testing and Yield Optimization- Hierarchical Multitask Learning for Wafer Quality Prediction- Co-clustering Structural Temporal Data from Semiconductor Manufacturing		
Module:5	**Learning from Limited Data in VLSI CAD**	**4 hours**
Introduction-Iterative Feature Search- Assumptions in Machine Learning- Traditional Machine Learning-An Adjusted Machine Learning View- A SAT-Based Implementation- Incorporating Domain Knowledge		
Module:6	**Machine Learning-Based System Optimization and Uncertainty Quantification for Integrated Systems**	**4 hours**
Introduction-Optimization Oriented Design Flow- Black-Box Optimization-Two-Stage Bayesian Optimization- Co-optimization of Embedded Inductor and Integrated Voltage Regulator-Uncertainty Quantification- Uncertainty Quantification of the IVR Efficiency		
Module:7	**Energy-Efficient Design of Advanced Machine Learning Hardware**	**8 hours**
Design Automation Flow, Physical Design and Optimization, Layout and Mask Data Preparation, Verification and Testing.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Stuart Russell and Peter Norvig, Artificial Intelligence: A Modern Approach, 2022, 4th Edition, Pearson Education, UK.
2.	Ibrahim M. Elfadel, Duane S. Boning, and Xin Li, Machine learning in VLSI Computer-Aided Design, 2019, 1st Edition, Springer.
Reference Books	
1.	Abhishek Kumar, Suman Lata Tripathi, and K. Srinivasa Rao, Machine Learning Techniques for VLSI Chip Design, 2023, 1st edition, Wiley-Scrivener.
2.	Laung-Terng Wang, Yao-Wen Chang, Kwang-Ting (Tim) Cheng, Electronic Design Automation: Synthesis, Verification, and Test (Systems on Silicon), 2009, 1st edition, Morgan Kaufmann.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz, and Final Assessment Test.			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD403L	Neuromorphic Computing	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

- Understand neuromorphic computational paradigms of intelligent systems.
- Understand the performance measure of information processing in neuromorphic systems.
- Design of Spiking Neural Networks depending on neuron and neural system models
- Design of Neuromorphic Systems for computation and machine learning.

Course Outcomes

After completion of the course, the student will be able to:

- Understand the analogy between the neuromorphic systems in nature and the brain inspired artificial intelligence.
- Understand the neuron models and spiking neural networks (SNN)
- Analyze the types of neural networks with reasoning, context, situation and intelligence in cognitive systems and their test methods.
- Have some knowledge on the Neuromorphic VLSI systems
- Impart high speed performance with necessary hardware modifications.
- Understanding how to implement SNN using various simulation platforms.

Module:1	Introduction to Neuromorphic Computation Systems	3 hours

Understanding of Neuromorphic Computing, Basic principles of Neuromorphic Computing, Difference from traditional computer architectures and computing paradigms.

Module:2	Neuromorphic System Design Fundamentals and Challenges	5 hours

Neural Networks- Artificial Neural Networks-Spiking Neural Networks-Learning in Spiking Neural Networks, Synapse Memory Technologies, Neurons Communication Network, System Design Domains, Spiking Neuron Models.

Module:3	Learning Paradigms	10 hours

Learning Algorithms-Supervised and unsupervised learning, Introduction to ANN architecture-Multilayer perceptron, Back propagation algorithm, Radial basis function network- Hetero association- Recurrent Neural networks- Hopfield networks- Competitive Learning neural networks, Self-Organizing Map, Learning Vector Quantization.

Module:4	Emerging Memory Devices for Neuromorphic Computing	7 hours

Memory Technology- SRAM- DRAM- STT- RAM- RRAM- Resistive Crossbar- Change Memory, Other Memory Technologies, Memory for Neuromorphic Systems,

Neuron State Memory, Dynamic NVM Synapse- Learning Related NVM- Conductance Drift in NVM.		
Module:5	**Neuromorphic Systems and Algorithms**	**5 hours**
Neuromorphic VLSI Systems, Neuromorphic Algorithms- Novel Learning Algorithms for Neuromorphic chips, Neuromorphic Sensors and Applications- Neuroelectronic Hybrid system.		
Module:6	**Hardware Accelerators and Machine Learning Algorithms**	**5 hours**
Hardware Accelerators for Machine Learning, Spike based Quasi Propagation, Machine Learning for IoT, Machine learning for Edge Computing.		
Module:7	**Neural Network Implementation using Python and Verilog**	**8 hours**
Construct Spiking Neural Networks, Simulate Spiking Neural Networks-using python and Verilog, Transform Spiking Neural networks, Visualize Spiking Neural Networks.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**

Text Book(s)

1.	Abderazek Ben Abdallah and Khanh N. Dang, Neuromorphic Computing Principles and Organization, 2022, 1st Edition, Springer, Cham, Switzerland.
2.	Khaled Salah Mohamed, Neuromorphic Computing and Beyond- Parallel, Approximation, Near Memory, and Quantum, 2020, 1st Edition, Springer, Cham, Switzerland.
3	Zheng, Nan, Learning in Energy-Efficient Neuromorphic Computing: Algorithm and Architecture Co-Design, 2020, 1st Edition, John Wiley & Sons.

Reference Books

1.	Paul Miller, An Introductory Course in Computational Neuroscience, 2018, Illustrated Edition, MIT Press, USA.
2.	Wulfram Gerstner, Werner M. Kistler, Richard Naud and Liam Paninski, Neuronal Dynamics, 2014, Illustrated Edition, Cambridge University Press, USA.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD405L	Hardware Security	3	0	0	3
Pre-requisite	BECE102L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Describe state-of-the-art hardware security techniques and justify their applications and limitations
2. Describe the threats against a system from hardware perspective and available countermeasures and apply the knowledge to choose an appropriate set of countermeasures for a certain threat assessment.
3. Explain the need of hardware security primitives and justify advantages and disadvantages with the different primitives and choose an appropriate primitive for a specific application

Course Outcomes

After completion of the course, the student will be able to:

- Understand the basics of hardware security for ICs, IPs and systems
- Design, optimize and implement block ciphers
- Learn the hardware security primitives and their classifications
- Acquire adequate knowledge on hardware IP protection and trust
- Familiarize malwares towards hardware security
- Understand the significance of trust zone in security architecture

Module:1	Fundamentals of hardware security for Integrated Circuits and Systems	3 hours

Introduction to hardware security, Hardware Security and trust, Attacks, Vulnerabilities and Countermeasures, Introduction to Block Ciphers

Module:2	Hardware Design of Cryptographic Algorithms and their Attacks	7 hours

Algorithmic and Architectural Optimizations for AES Design- Hardware Implementations for Block Ciphers-Parallel Architecture, Loop Architecture, Pipeline Architecture, Side Channel Analysis-Introduction to Side Channel Analysis, Passive and Active Noninvasive Physical Attacks, Side-Channel Attacks-power, EM, timing and fault attacks

Module:3	Hardware Security Primitives	7 hours

Physically Unclonable Functions (PUFs)- PUF Preliminaries, PUF Classifications, Common PUF Architectures, PUF Applications, True random number generation (TRNG)- TRNG Preliminaries, Common TRNG Architectures, TRNG Applications

Module:4	Hardware Intellectual Property Trust & Test	8 hours

Security and Trust Vulnerabilities in Third-Party IPs , Security Rule Check, Digital Circuit Vulnerabilities to Hardware Trojans, Test-oriented attacks- Scan-Based Attacks, JTAG-Based Attacks

Module:5	Hardware Trojans in IP cores and ICs	6 hours

Hardware Trojan Nomenclature and Operating Modes, Countermeasures Such as Design and Manufacturing Techniques to Prevent/Detect Hardware Trojans, Logic Testing and Side-channel Analysis based Techniques for Trojan Detection, Circuit Vulnerabilities to Hardware Trojans.		
Module:6	**Counter measures**	**7 hours**
Side-channel resistant designs -SCA countermeasures, FA countermeasures (Fault-tolerance of Cryptographic Hardware), IP Encryption, Logic Obfuscation, Hardware Watermarking, IC Metering PUF-Based Authentication.		
Module:7	**Design for Security -Trust Zone**	**5 hours**
Impact of Hardware Security Compromise on Public Infrastructure -Design for Hardware Trust, Security Architecture- SAMSUNG KNOX,INTEL SGX, ARM (Trust zone)		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**
Text Book(s)		
1.	Swarup Bhunia, Mark Tehranipoor, Hardware Security: A Hands-on Learning Approach, 2018, 1st edition, Morgan Kaufmann Publishers.	
2.	Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, Hardware Security: Design, Threats, and Safeguards, 2015, 1st edition, CRC Press.	
Reference Books		
1.	Kazuo Sakiyama, Yu Sasaki, Yang Li, Security of Block Ciphers: From Algorithm Design to Hardware Implementation, 2015, 1st edition, Wiley.	
2.	Mark Tehranipoor, Prabhat Mishra, Swarup Bhunia (Eds.), Hardware IP Security and Trust, 2017, 1st edition, Springer.	
3.	Stefan Mangard, Elisabeth Oswald, Thomas Popp: Power analysis attacks - revealing the secrets of smart cards. 2007, 1st edition, Springer.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.		
Recommended by Board of Studies	05-11-2024	
Approved by Academic Council	No. 76	Date 27-11-2024

Course Code	Course Title	L	T	P	C
BEVD406L	High Speed Interconnects for VLSI Design	3	0	0	3
Pre-requisite	BECE303L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

- Gain knowledge on VLSI Interconnects & Modeling.
- Understand interconnect delays and transmission line parameters.
- Classify and understand problems/solutions of novel interconnects.
- Explore the characteristics of advanced materials such as Graphene for use in high-speed interconnects.

Course Outcomes

After completion of the course, the student will be able to:

- Understand the basics of VLSI Interconnects, parasitic parameters
- Analyze on interconnect delay, frequency loss and modeling requirements
- Investigate origin of several interconnect effects and explore techniques for electromagnetic and circuit modeling of these interconnect effects.
- Explore into cross talk – Analysis & Reduction
- Analyze futuristic interconnects
- Identify industry issues and find solutions

Module:1	Basics of VLSI Interconnects	4 hours

Interconnections for VLSI Applications- Metallic Interconnections- Distributed RC interconnect model, Elmore delay- Elmore delay in interconnects- Elmore delay in RC tree and branched interconnects.

Module:2	Parasitic Resistances, Capacitances and Inductances	6 hours

Parasitic Resistances- General Considerations, Parasitic Inductances- General Considerations, Types- Self, Mutual and other types, Approximate Formulas for Capacitances- Parallel plate capacitance- Fringing Capacitance- Coupling Capacitance, Other methods of Capacitance Extraction.

Module:3	Interconnection Delays	6 hours

Metal-Insulator- Semiconductor Microstrip Line Model of an Interconnection, Transmission Line Analysis of Single Level Interconnections- Transmission Line Analysis of Parallel Multilevel Interconnections- Analysis of Crossing Interconnections, Very High Frequency Losses in a Microstrip Interconnection, Compact Expressions for Interconnection Delays, Interconnection Delays in Multilayer Integrated Circuits, Active Interconnections.

Module:4	Modeling of Interconnects	8 hours

Equivalent Elmore model for RLC interconnects (Distributed model), Two-pole model of RLC interconnects from ABCD parameters, Simulation of RLC interconnects, Equivalent circuit to simulate skin effect, Thermal modeling with equivalent electrical circuit, Analysis of coupled interconnects- Simulation of RC coupled interconnects,

Estimation of interconnect parameters from S parameters.		
Module:5	**Cross Talk Analysis**	**7 hours**
Matrix formulation of coupled interconnects, Coupled RLC interconnects, Decoupling of interconnects by diagonalization of matrix, Lumped capacitance approximation Modeling of coupled transmission lines, Reducing cross talk- Techniques for mitigation of cross- talk, Cross-talk and timing jitters in two identical interconnects- Effects of cross-talk and timing jitters.		
Module:6	**Modeling Interconnect parameters**	**6 hours**
Quantum properties, Quantum Conductance, Capacitance, Kinetic Inductance, Diameter dependent modeling of CNT Interconnects, Resistance Models, Transmission Line Interconnect Models.		
Module:7	**Novel Interconnects**	**6 hours**
Optical interconnects- Carbon Nano tubes- Graphene nano ribbons- Copper wires, Superconducting interconnects, Nanotechnology interconnects, Silicon nano wires, System issues, Design and Material aspects		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**
Text Book(s)		
1	Ashok K. Goel, High-Speed VLSI Interconnections, 2015, 2nd Edition, Wiley Publishers, Hoboken, USA.	
2.	Brajesh K. Kaushik, Manoj K. Majumder, Carbon Nanotube Based VLSI Interconnects: Analysis and Design, 2015, 1st Edition, Springer India	
Reference Books		
1	H.B.Bakoglu, Circuits Interconnections and Packaging for VLSI, 1990, Illustrated Edition, Addison Wesley Publishing Company, USA.	
2	C.K.Cheng, J.Lillis, S.Lin and N.Chang, Interconnect Analysis and Synthesis, 2008, 1 st Edition, Wiley- Interscience, USA.	
3	J.M.Wang and E.S.Kuh, Recent Development in Interconnect Modeling, In: H.Grabinski (Eds)- Interconnects in VLSI Design, 2000, Springer, Boston, USA.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.		
Recommended by Board of Studies	05-11-2024	
Approved by Academic Council	No. 76	Date 27-11-2024

Course Code	Course Title	L	T	P	C
BEVD407L	Stacked IC Design	3	0	0	3
Pre-requisite	BECE303L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Introduce the students with issues in deep submicron CMOS design.
2. Acquaint the students with 3-D IC technology and its packaging techniques.
3. Equip the students with the knowledge on manufacturing technologies for 3-D IC.
4. Familiarize the students with TSV, its electrical properties and fabrication methods.
5. Impart knowledge on the physical design aspects of 3-D ICs.

Course Outcomes

After completion of the course, the student will be able to:

- Interpret the issues in deep submicron CMOS design.
- Understand the 3-D Technology and Packaging Techniques.
- Apprehend the manufacturing technologies for 3-D ICs.
- Understand the electrical properties and fabrication of TSV.
- Realize the physical design and thermal modeling for 3-D ICs.
- Investigate the power delivery for 3-D ICs.

Module:1	Issues in Deep Submicron CMOS Design	6 hours

Scaling issue, Interconnect issues, Mixed Signal Design of Deep Submicron Devices- ESD reliability of Deep Submicron Devices, Power Dissipation and Thermal problems, Design of Heat Sinks for Deep submicron IC's.

Module:2	3-D Technology and Packaging Techniques	6 hours

Silicon Interposer Technology, Through Silicon Vias (TSVs), Hybrid packaging technique, Silicon-Less Interconnect Technology, 3D Integrated Architectures.

Module:3	Manufacturing Technologies for 3-D IC	6 hours

Monolithic 3-D IC: Laser Crystallization, Double-Gate MOSFET for stacked 3-D ICs, 3-D ICs with TSV- Wafer level integration, Contactless 3-D ICs.

Module:4	Electrical Properties of Through Silicon Vias	5 hours

Physical characteristics of TSV, Electrical model of TSV, Modeling a 3-D via as a Cylinder, Compact models (R, L, G, C).

Module:5	Materials and Fabrication of TSV	7 hours

CNT, GNR, Properties of TSVs, Fabrication of TSVs, Challenges for TSV Implementation, Modeling and Performance Analysis of Copper-based, CNT-based, GNR-based TSVs, Liners in TSV.

Module:6	Thermal Modeling for 3-D ICs	7 hours

Heat Transfer in Three-Dimensional ICs, Thermal Analysis Techniques, Thermal Management Through Power Density Reduction - Enhanced Thermal Conductivity,

Hybrid Methodologies for Thermal Management.		
Module:7	**Power Delivery for 3-D ICs**	**6 hours**
The Power Delivery Challenge, Models for Three-Dimensional Power Distribution Networks, Through Silicon Via Technologies to Mitigate Power Supply Noise, Wire Sizing Methods in Three-Dimensional Power Distribution Networks.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture Hours:	**45 hours**

Text Book(s)	
1.	Vasilis F. Pavlidis, LLoannis Savidis and Eby G. Friedman, Three-Dimensional Integrated Circuit Design, 2017, 2nd Edition, Elsevier Science, Netherlands.
2.	B. Wu, A. Kumar and S. Ramaswami, 3D IC Stacking Technology, 2011, 1st Edition, McGraw-Hill Education, USA.
Reference Books	
1.	Rohit Sharma, Design of 3D Integrated Circuits and Systems, 2015, 1st Edition, CRC Press, USA.
2.	J. Lau, Through-Silicon Vias for 3D Integration, 2012, Illustrated Edition, McGraw Hill, USA.
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.	

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BEVD408L	Verification Methodologies	3	0	0	3
Pre-requisite	BEVD205L, BEVD205P	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Provide an understanding and the need of functional verification.
2. Develop constrained random verification environment with assertions and coverage.
3. Write reusable verification environment using UVM.
4. Provide an understanding of CDC and LP Verification

Course Outcomes

After completion of the course the student will be able to:

1. Develop Constrained Random Verification Environment.
2. Perform Functional Coverage and Assertions.
3. Understand Threads and IPC.
4. Develop UVM based test environment.
5. Develop Verification Environment for Standard Protocol.
6. Perform CDC and LP Verification.

Module:1	Functional Verification	5 hours

Introduction, Functional Verification challenges and solutions, System Verilog Paradigm, Review of System Verilog, Constrained Random Verification Environment.

Module:2	Functional Coverage and Assertions	7 hours

Coverage Types – Anatomy of covergroup – Triggering a covergroup, Data Sampling – Cross Coverage – Coverage options, Evolution of System Verilog Assertions– Advantages – Creating an assertion testplan – SVA Assertion Methodology – Immediate Assertions – Concurrent Assertions, Clocking Basics – Operators – SVA Applications.

Module:3	Threads, IPC and Advanced OOPS	5 hours

Working with Threads - Interprocess communication – Events, Semaphores, Mailboxes – Building a testbench with Threads and IPC - Callbacks, Parameterized Classes, Static and singleton classes, Creating a Test registry.

Module:4	UVM	6 hours

UVM Hierarchy – UVM Class Library – UVM Transaction Level Communication Protocol – UVM Phases.

Module:5	UVM – Verification Environment	6 hours

Developing reusable verification components– Using Verification components– Developing reusable verification environment– UVM Examples.

Module:6	Case Study	8 hours

Verification of Standard Protocol– AMBA AHB-UVM Based.

Module:7	**Clock Domain Crossing and Low Power Verification**	**6 hours**
Design Complexity and CDC–Metastability– Synchronizer– CDC Checks using SVA– CDC Verification Methodology– CDC Verification at gate level– EDA Vendors and CDC Tools support– Power Requirements– Dynamic Low Power Verification challenges, UPF– UPF Methodology– UPF– Detailed SoC Example– Power Estimation at Architecture Level– UPF Features Subset.		
Module:8	**Contemporary Issues**	**2 hours**
Guest lecture from Industries and R & D Organizations.		
	Total hours:	**45 hours**

Text Book(s)

1.	Ashok B. Mehta, ASIC/SoC Functional Design Verification – A Comprehensive guide to Technologies and Methodologies, 2017, 1st Edition, Springer.
2.	Christian B Spear, System Verilog for Verification: A guide to learning the Testbench language features, 2012, 3rd Edition, Springer Publications.

Reference Books

1.	Progyna Khondkar, Low-Power Design and Power Aware Verification, 2017, 1st Edition, Springer.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test			
Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course code	Course Title	L	T	P	C
BEVD409L	Advanced Semiconductor Devices	3	0	0	3
Pre-requisite	BEVD201L	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Give in-depth knowledge of the structure and operation of advanced semiconductor devices.
2. Give students an idea about the properties of advanced materials used for semiconductor device fabrication.
3. Introduce the applications of advanced semiconductor devices.
4. Discuss the design challenges related to advanced semiconductor devices

Course Outcomes

After completing this course, students shall be able to:

1. Understand the physics of Nanoscale Multi-Gate Devices and identify the related design challenges
2. Understand the operation of LED, LASER, and gain knowledge of their applications.
3. Gain knowledge of power MOSFETs, Tunnel FETs and their applications
4. Understand the operation of semiconductor-based sensors and their IoT and AI-based applications
5. Gain knowledge of basic principles and developments related to Ferroelectric Transistors
6. Analyze the design, synthesis, and performance of organic semiconductor devices.

Module:1	Nanoscale Multi Gate Devices	7 hours
Evolution from planar to nonplanar devices, Multigate Transistors – Multigate Transistor Physics – Gate All Around Transistor – Stacked Nanosheet Field Effect Transistor – Design Challenges, FinFET – Device Structure – Characteristics		
Module:2	**Optoelectronic Devices**	**6 hours**
Light Emitting Devices – Light emitting diodes (III-V, Quantum, Organic LEDs) and Light Emitting Transistors, Semiconductor LASERs, and applications, Photonic Devices.		
Module:3	**Power MOSFET**	**6 hours**
Ideal Specific On-Resistance – Device Structure and Operation – Blocking Voltage – Forward conduction characteristics –Cell Optimization – Output Characteristics		
Module:4	**Ferroelectric Transistors**	**6 hours**
Features, Principles, and Developments of Ferroelectric-Gate Field-Effect Transistors-Switching in Nanoscale Hafnium Oxide-Based Ferroelectric Transistors		
Module:5	**Semiconductor Devices for sensors**	**5 hours**
Semiconductor-based sensors (Gas sensors, Thermal sensors, Chemical sensors, pressure sensors) and their utilization for IoT and AI applications		
Module:6	**Steep Slope Devices**	**7 hours**
Basics of tunnel field effect transistors (FET), III-V Tunnel FET, Carbon-based tunnel FET, Nanowires tunnel FET, Application of tunnel FET, Introduction to negative capacitance FET and Impact ionization FET		
Module:7	**Organic Semiconductor Devices**	**6 hours**

Theoretical Aspects of Charge Transport in Organic Semiconductors: A Molecular Perspective – Charge Transport in Oligomers – Charge Transport Physics of Solution process, Organic Light Emitting Diode (OLEDs) – Device Physics – Characteristics, Processed Organic Field-Effect Transistors – Design and Transistor Performance of Organic Semiconductors- OFET, Organic solar cells.		
Module:8	**Contemporary Topics:**	**2 hours**
Guest lecture from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**
Text Book(s)		
1.	S. M. Sze and M. K. Lee, Semiconductor Devices Physics and Technology, 2016, 3rd Edition, John Wiley.	
2.	Mark S Lundstorm and Jing Guo, Nanoscale Transistors Device Physics, Modeling and Simulation, 2006, 1st edition, Springer.	
Reference Books		
1.	B. Jayant Baliga, Fundamentals of Power Semiconductor Devices, 2019, 2nd edition, Springer.	
2.	Byung-Eun Park, Hiroshi Ishiwara, Masanori Okuyama, Shigeki Sakai, Sung-Min Yoon, Ferroelectric-Gate Field Effect Transistor Memories Device Physics and Applications, 2018, 2nd edition, Springer.	
3.	Zhenan Bao and Jason Locklin, Organic Field effect transistor, 2022, 1st edition, CRC Press.	
4.	S.M Sze, Semiconductor Sensors, 1994, 1st edition, John Wiley.	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.		
Recommended by Board of Studies	05-11-2024	
Approved by Academic Council	No. 76	Date 27-11-2024

Course code	Course Title	L	T	P	C
BEVD410L	Introduction to MEMS	3	0	0	3
Pre-requisite	NIL	Syllabus Version			
		1.0			

Course Objectives

This course is aimed to:

1. Educate on various Micro fabrication techniques.
2. Introduce various sensors and actuators
3. Educate on the applications of MEMS integrated with VLSI

Course Outcome

After completion of the course, the student will be able to:

1. Understand the concepts of micro sensors and actuators
2. Comprehend the basic governing laws of miniaturization.
3. Understand the materials requirement and different fabrication process of MEMS devices.
4. Obtain knowledge of various modeling and simulation techniques for MEMS.
5. Demonstrate CMOS based Micro system.
6. Know the importance of reliability studies and Packaging of MEMS.

Module:1	Sensors	6 hours

Micro sensors - Basic principles and working of micro sensors- Acoustic wave micro sensors- Bio-medical micro sensors- Chemical micro sensors – Optical Sensors – Pressure micro sensors- Thermal micro sensors-acceleration micro sensors

Module:2	Actuators	6 hours

Micro actuators - Basic principles and working of micro actuators- Electrostatic micro actuators- Piezoelectric micro actuators- Thermal micro actuators- SMA micro actuators- Electromagnetic micro actuators, micro valves, micro pumps.

Module:3	Scaling Laws of miniaturization	6 hours

The multi-disciplinary nature of MEMS, Smart materials, Structures and Systems, Scaling in Geometry-Scaling in Rigid-Body Dynamics-Scaling in Electrostatic Forces-Scaling in

Electromagnetic Forces-Scaling in Electricity-Scaling in Fluid Mechanics-Scaling in Heat Transfer

Module:4	Materials and Fabrication	7 hours

Substrates and wafers, Silicon and Silicon compounds, Gallium Arsenide, Piezoelectric materials, Polymers. Micro system fabrication process- Lithography, Dry and wet etching, Film deposition (PVD, CVD), LIGA, Micromolding, Electro-deposition.

Module:5	Modeling and Simulation of MEMS Devices	7 hours

Introduction to MEMS modeling and simulation tools, Basic concepts of design of MEMS devices and processes, Design for fabrication, Other design considerations, Analysis of MEMS devices, FEM and Multiphysics analysis, Modeling and simulation, connection between molecular and continuum mechanics.

Module:6	CMOS – MEMS	6 hours

CMOS technology, Classification of CMOS MEMS Technology, Fabrication methods, Read out circuits, Examples of CMOS sensors

Module:7	**Packaging, Integration and reliability**	**5 hours**
Requirements of Packaging, Integration of MEMS – VLSI Technology, MEMS Packaging/ Package Types/ Packaging Unit Processes. MEMS Flip Chip Bonding, MEMS Testing, Reliability & Failure Analysis		
Module:8	**Contemporary Issues**	**2 hours**
Guest lectures from Industries and R & D Organizations		
	Total Lecture hours:	**45 hours**

Text Book(s)

1.	Tai-Ran-Hsu, MEMS and Microsystems: Design, Manufacture, and Nanoscale Engineering,2020, 2nd edition, McGraw Hill.
2.	Chang Liu, Foundation of MEMS, 2012, 2nd edition, Pearson Education.

Reference Books

1.	Sergey Edward Lyshevski, Nano- and Microelectromechanical Systems, Fundamentals of Nano- and Microengineering, 2nd edition, 2000, CRC Press.
2.	Marc Madou, Fundamentals of Microfabrication: The Science of Miniaturization, 2nd edition, 2017, CRC Press.
3.	V. Choudhary, K. Iniewski, MEMS: Fundamental Technology and Applications, 2017, 1st edition, CRC Press.
4.	Mohamed Gad el- Hak, The MEMS Hand book, 2012, 1st edition, CRC Press.

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz and Final Assessment Test.

Recommended by Board of Studies	05-11-2024		
Approved by Academic Council	No. 76	Date	27-11-2024

Course Code	Course Title	L	T	P	C
BECE399J	Summer Industrial Internship	0	0	0	1
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

1. The course is designed so as to expose the students to industry environment and to take up on-site assignment as trainees or interns.

Course Outcomes

1. Demonstrate professional and ethical responsibility.
2. Understand the impact of engineering solutions in a global, economic, environmental and societal context.
3. Develop the ability to engage in research and to involve in life-long learning.
4. Comprehend contemporary issues.

Module Content	**4 Weeks (28 hours)**
Four weeks of work at industry site. Supervised by an expert at the industry.	

Mode of Evaluation: Internship Report, Presentation and Project Review

Recommended by Board of Studies	12-10-2022		
Approved by Academic Council	No. 68	Date	19-12-2022

Course Code	Course Title	L	T	P	C
BECE497J	Project-I	0	0	0	3
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

1. To provide sufficient hands-on learning experience related to the design, development and analysis of suitable product / process so as to enhance the technical skill sets in the chosen field.

Course Outcomes

1. Demonstrate professional and ethical responsibility.
2. Evaluate evidence to determine and implement best practice.
3. Mentor and support peers to achieve excellence in practice of the discipline.
4. Work in multi-disciplinary teams and provide solutions to problems that arise in multi-disciplinary work.

Module Content **(Project Duration: One Semester)**

Project may be a theoretical analysis, modeling & simulation, experimentation & analysis, prototype design, fabrication of new equipment, correlation and analysis of data, software development, applied research and any other related activities.

Can be individual work or a group project, with a maximum of 3 students.

In case of group projects, the individual project report of each student should specify the individual's contribution to the group project.

Publications in the peer reviewed journals / International Conferences will be an added advantage.

Mode of Evaluation: Assessment on the project - project report to be submitted, presentation and project reviews.

Recommended by Board of Studies	12-10-2022		
Approved by Academic Council	No. 68	Date	19-12-2022

Course Code	Course Title	L	T	P	C
BECE498J	Project-II / Internship	0	0	0	5
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

1. To provide sufficient hands-on learning experience related to the design, development and analysis of suitable product / process so as to enhance the technical skill sets in the chosen field.

Course Outcomes

1. Formulate specific problem statements for ill-defined real life problems with reasonable assumptions and constraints.
2. Perform literature search and / or patent search in the area of interest.
3. Conduct experiments / Design and Analysis / solution iterations and document the results.
4. Perform error analysis / benchmarking / costing.
5. Synthesize the results and arrive at scientific conclusions / products / solution.
6. Document the results in the form of technical report / presentation.

Module Content **(Project Duration: One Semester)**

1. Project may be a theoretical analysis, modeling & simulation, experimentation & analysis, prototype design, fabrication of new equipment, correlation and analysis of data, software development, applied research and any other related activities.
2. Project can be for one or two semesters based on the completion of required number of credits as per the academic regulations.
3. Can be individual work or a group project, with a maximum of 3 students.
4. In case of group projects, the individual project report of each student should specify the individual's contribution to the group project.
5. Carried out inside or outside the university, in any relevant industry or research institution.
6. Publications in the peer reviewed Journals / International Conferences will be an added advantage.

Mode of Evaluation: Assessment on the project - project report to be submitted, presentation and project reviews.

Recommended by Board of Studies	12-10-2022		
Approved by Academic Council	No. 68	Date	19-12-2022