VIT®

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)

SCHOOL OF ELECTRONICS ENGINEERING

B.Tech - Electronics Engineering

(VLSI Design and Technology)

(B.Tech - BVD)

Curriculum

(*2026-2027 admitted students*)

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B.Tech - Electronics Engineering (VLSI Design and Technology)

PROGRAMME EDUCATIONAL OBJECTIVES (PEOs)

PEO1. **(Technical knowledge):** Graduates will have a sound knowledge on the fundamentals of mathematics, science, and electronics enabling them to analyse, design and test integrated circuits and systems.

PEO2. **(Professional growth / career):** Graduates will embrace their capability to expand horizons beyond engineering for academia, research, innovation and entrepreneurship.

PEO3. **(Soft skills):** Graduates will demonstrate their professional and ethical responsibilities with team spirit and engage in life-long learning.

PROGRAMME SPECIFIC OUTCOMES (PSOs)

PSO1: Develop electronic circuits and systems with electronic materials to contribute for the global semiconductor ecosystem.

PSO2: Design, implement and test analog and digital integrated circuits and systems.

PSO3: Apply and develop the state of the art industry standard Electronic Design Automation for societal needs.

Category Credit Detail			
Sl.No.	**Description**	**Credit**	**Maximum Credit**
1	NC - Non Credit Course	2	2
2	UCC - University Core Courses	60	60
3	PCC - Programme Core Courses	40	40
4	CON - Concentration	20	20
5	OEC - Open Elective Courses	40	40
Total Credits		160	

Non Credit Course									
sl.no	**Course Code**	**Course Title**	**Course Type**	**Version**	**L**	**T**	**P**	**J**	**Credit**
1	BAENG100	Effective English Communication	Lab Only	1.0	0	0	4	0	2.0

University Core Courses									
sl.no	**Course Code**	**Course Title**	**Course Type**	**Version**	**L**	**T**	**P**	**J**	**Credit**
1	BACHY101	Environmental Sciences	Online Course	1.0	0	0	0	0	2.0
2	BACHY107	Applied Chemistry for Electronics Engineering	Embedded Theory and Lab	1.0	3	0	2	0	4.0
3	BACSE101	Problem Solving using Python	Lab Only	1.0	0	0	4	0	2.0
4	BACSE102	Problem Solving using Java	Lab Only	1.0	0	0	4	0	2.0
5	BAECE191	Basic Multidisciplinary Project	Project	1.0	0	0	0	0	2.0
6	BAEEE101	Basic Engineering	Embedded Theory and Lab	1.0	3	0	2	0	4.0
7	BAENG101	Technical English Communication	Embedded Theory and Lab	1.0	3	0	2	0	4.0
8	BAFLC100	Foreign Language	Basket	1.0	0	0	0	0	2.0
9	BAHUM101	India Studies	Online Course	1.0	0	0	0	0	1.0
10	BAMAT101	Multivariable Calculus and Differential Equations	Embedded Theory and Lab	1.0	3	0	2	0	4.0
11	BAMAT201	Complex Variables and Linear Algebra	Theory Only	1.0	3	1	0	0	4.0
12	BAPHY108	Semiconductor Physics	Embedded Theory and Lab	1.0	3	0	2	0	4.0

Programme Core Courses									
sl.no	**Course Code**	**Course Title**	**Course Type**	**Version**	**L**	**T**	**P**	**J**	**Credit**
1	BAECE103	Network Theory	Theory Only	1.0	3	1	0	0	4.0
2	BAECE202	Engineering Electromagnetics	Theory Only	1.0	3	1	0	0	4.0

Programme Core Courses									
3	BAECE204	Microcontrollers and Embedded C Programming	Embedded Theory and Lab	1.0	3	0	2	0	4.0
4	BAECE205	Control Systems	Theory Only	1.0	3	1	0	0	4.0
5	BAEVD101	Electronic Devices	Embedded Theory and Lab	1.0	3	0	2	0	4.0
6	BAEVD102	Digital System Design	Embedded Theory and Lab	1.0	3	0	2	0	4.0
7	BAEVD201	Electronic Circuits	Embedded Theory and Lab	1.0	3	0	2	0	4.0
8	BAEVD202	Computer Architecture	Theory Only	1.0	3	1	0	0	4.0
9	BAEVD203	Communication Systems	Theory Only	1.0	3	1	0	0	4.0
10	BAEVD204	Signal Processing	Embedded Theory and Lab	1.0	3	0	2	0	4.0

Concentration									
sl.no	Course Code	Course Title	Course Type	Version	L	T	P	J	Credit
1	BABVD001	VLSI Design and Technology	Basket	1.0	0	0	0	0	20.0
2	BABVD002	VLSI System Design and Testing	Basket	1.0	0	0	0	0	20.0
3	BABVD003	VLSI Devices and Technology	Basket	1.0	0	0	0	0	20.0

Open Elective Courses									
sl.no	Course Code	Course Title	Course Type	Version	L	T	P	J	Credit
1	BAESP201	Spanish Level II	Embedded Theory and Lab	1.0	2	0	2	0	3.0
2	BAEVD311	VLSI Architectures dor Signal Processing	Theory Only	1.0	3	1	0	0	4.0
3	BAEVD312	Semiconductor Optoelectronic Devices	Embedded Theory and Lab	1.0	3	0	2	0	4.0
4	BAEVD313	Hardware Accelerators for ML Applications	Theory Only	1.0	3	1	0	0	4.0
5	BAFRE201	French for Engineers: Language and Communication Lab	Embedded Theory and Lab	1.0	2	0	2	0	3.0
6	BAGER201	German Level II	Embedded Theory and Lab	1.0	2	0	2	0	3.0
7	BAHIN101	Prathamik Hindi	Theory Only	1.0	3	0	0	0	3.0
8	BAHIN102	Prayojanmulak Hindi	Embedded Theory and Lab	1.0	2	0	2	0	3.0
9	BAJAP201	Japanese Level II	Embedded Theory and Lab	1.0	2	0	2	0	3.0
10	ULINK100	Undergraduate Lab Integration for Knowledge & Innovation	Basket	1.0	0	0	0	0	3.0

Course code	Course title	L	T	P	C
BAEEE101	**Basic Engineering**	3	0	2	4
Pre-requisite	NIL	Syllabus version			
		1.0			

Course Objectives

- To introduce fundamental principles of major engineering disciplines.
- To create awareness of interdisciplinary engineering systems and their applications

Course Outcomes

At the end of the course students will be able to

1. Analyse the electrical circuits, electrical motors and the role of power electronics in industrial applications.
2. Acquire foundational knowledge of electronic devices and communication systems.
3. Apply BIS standards to create basic 2D and 3D representations of engineering components.
4. Explain the fundamental principles and applications of manufacturing processes, energy conversion systems, and mechanical automation technologies.
5. Analyse real-world examples where bio-inspired solutions have led to breakthroughs in engineering.

Module:1	**Principles of Electrical Engineering: Circuits and Power conversion equipment**	**12 hours**

Electric circuit components, Mesh current analysis, Node voltage analysis, Thevenin's and Superposition theorems, Single phase AC circuits- RL, RC, RLC, Power and Energy Calculations, Power Factor, Basics of Electrical Safety and Earthing.

Introduction to electro mechanical energy conversion, principle of operation of Electrical Machines - DC Motor, Induction motors, BLDC Motor and single phase Transformer, Concepts of Power Electronics and Industrial Applications of Electrical Drives (Qualitative Analysis)

Module:2	**Foundations of Electronics and Communication systems: Devices, Circuits, and Systems**	**8 hours**

Characteristics of PN Junction Diode, Zener Diode, BJT and MOSFET. Rectifiers and Voltage Regulators. Introduction to Operational Amplifiers. Electromagnetic Specturm. Elements of Communication Systems. Overview of cellular communication. Fundamentals of Satellite Communication and Radar.

Module:3	**Engineering Graphics and CAD**	**9 hours**

Introduction to Engineering Drawing – Importance and scope of engineering graphics, BIS standards for lines, lettering and dimensioning. Orthographic Projections – Principles of projection, first angle and third angle projections. Introduction to Projection of Solids- Isometric Projections and perspective projections. Freehand Sketching – Sketching of simple machine components and objects. Drawing of a simple residential floor plan as per IS SP7, Introduction to CAD.

Module:4	**Manufacturing Processs, Energy conversions and Mechanical Automation**	**9 hours**

Basic Metal Casting, Forming, Joining and Cutting Processes - Introduction to CNC Machining. Additive Manufacturing (3D Printing): Principles and Applications.

Fundamentals of Thermal engineering systems, Internal Combustion Engine. Introduction to Power Plants. Introduction to Refrigeration and Air Conditioning. Basics of Fuel Cells and Sustainable Energy Technologies. Introduction to Mechanisms - Four-bar mechanism and its inversions- Hexapod mechanisms. Mechanical Components and Motion Control in mechanical systems. Introduction to Robotics and Automation – Pneumatic and hydraulic actuators.		
Module:5	**Bio-Inspired Design in Engineering**	**5 hours**
Introduction to Biomimicry- Core principles. Case Studies Across Disciplines: Velcro inspired by burrs, self-healing materials based on skin regeneration -Termite mound-inspired ventilation systems in green buildings-Insect-inspired drones and soft robotics-Neural networks based on the human brain -Identify a problem and brainstorm a bio-inspired solution.		
Module: 6	**Contemporary Topics**	**2 hours**
Lectures by Industry or Research experts		
	Total Lecture hours:	**45 hours**

Text Book(s)	
1.	Allan R. Hambley, "Electrical Engineering -Principles & Applications", 2019, 6th Edition, Pearson Education
2	R.L. Boylestad and L. Nashelsky, "Electronic Devices and circuit theory", 11th Edition, person Publications
3	Louis E Frenzel Jr, "Principles of Electronics Communication Systems", 2016, McGraw Hill Eduation.
4	Bhatt N. D., Engineering Drawing, Charotar Publishing House Pvt. Ltd, 2019.
Reference Books	
1.	John bird, "Electrical Circuit Theory and Technology", 4th edition, Newnes Publications, Elsevier, 2010
2.	George Kennedy,Brendan Davis, Srm Prasanna "Electronic Communication Systems", McGraw Hills, 2011
3.	Serope Kalpakjian, and Steven Schmid, Manufacturing Engineering and Technology, 2020, 8th edition, Pearson education.
4.	Nag P. K., Basic & Applied Thermodynamics, 2009, 2nd Edition, McGraw Hill Education.
5.	Rattan S. S, Theory of Machines, Tata McGraw Hill, 2019
6.	Craig, John. J. (2008), Introduction to Robotics: Mechanics and Control, Second Edition, Pearson Education, New Delhi.

List of Lab Experiments (Electrical and Electronics Engineering)

1. Verification of KCL and KVL in an Electrical Circuit
2. Verification of Mesh and Nodal Analysis in an Electrical Circuit
3. Time domain analysis of a single phase series RL Circuit
4. Measurement of Power and power factor in a single phase RL Circuit using 3- volt meter method
5. Speed Control of a PMDC Motor with DC-DC Buck Converter
6. Measurement of Earth Resistance using an Meggar

7. Analysis of a Zener Diode Voltage Regulator
8. Single-Phase Full-Wave Diode Rectifier with Resistive Load
9. Design and Testing of a Light Dimmer Circuit Using a Darlington Pair.
10. Create a 2D profile using basic sketch tools and apply appropriate geometric and dimensional constraints.
11. Develop a simple 3D solid model using features such as extrude, revolve, cut, fillet, chamfer, and shell.
12. Generate detailed 2D engineering drawings of simple parts from 3D solid models, including multiple views, dimensions, and annotations.

Mode of Evaluation: CAT, Assignment, Quiz, Seminar, Project, FAT			
Recommended by Board of Studies	23-05-2025		
Approved by Academic Council	No. 78	Date	12-06-2025

Course Code	Course Title	L	T	P	C
BAECE103	Network Theory	3	1	0	4
Pre-requisite	Nil	Syllabus Version			
		1			

Course Objectives

1. Familiarize with various circuit laws and theorems to solve DC and AC circuits
2. Understand advanced mathematical methods such as the Laplace transform and graph theory for solving circuit problems
3. Develop the ability to analyze the two-port networks, first and second-order circuits.

Course Outcomes

1. Compute DC circuit parameters using circuit laws and theorems
2. Determine the natural and step responses of RC, RL, and RLC circuits
3. Apply appropriate techniques and theorems for sinusoidal steady-state analysis
4. Apply the Laplace transform to circuits for steady-state and transient analysis
5. Compute two-port network parameters and network graph matrices for circuit analysis

Module:1	DC Circuit Analysis and Theorems	9 hours

Basic Circuit Elements and Sources; Ohm's Law; Kirchhoff's Laws; Series Resistors and Voltage Division; Parallel Resistors and Current Division; Wye-Delta Transformations; Methods of Analysis-Nodal Analysis, Mesh Analysis; Theorems-Superposition Theorem, Source Transformation Theorem, Thevenin's Theorem, Norton's Theorem, Maximum Power Transfer Theorem, Reciprocity Theorem.

Module:2	Transient Analysis of First and Second-Order Circuits	9 hours

First-Order Circuits- Source-Free RC Circuit, Source-Free RL Circuit, Singularity Functions, Step Response of an RC Circuit, Step Response of an RL Circuits; Second-Order Circuits- Source-Free Series RLC Circuit, Source-Free Parallel RLC Circuit, Step Response of a Series RLC Circuit, Step Response of a Parallel RLC Circuit, General Second-Order Circuits.

Module:3	Sinusoidal Steady State Analysis	9 hours

Sinusoids; Phasors; Phasor Relationships for Circuit Elements; Impedance and Admittance; Kirchhoff's Laws in the Frequency Domain; Instantaneous and Average Power; Complex Power; Methods of Analysis-Nodal Analysis, Mesh Analysis; Theorems-Superposition Theorem, Source Transformation Theorem, Thevenin's Theorem, Norton's Theorem, Maximum Average Power Transfer Theorem.

Module:4	Circuit Analysis in the S-domain	9 hours

Circuit Element Models; Circuit Analysis with and without initial conditions; Transfer Functions; From Laplace to Fourier Transform- Frequency Domain Analysis of Linear Circuits; Passive Filters- Lowpass Filter, High Pass Filter, Bandpass Filter, Band Stop Filter.		
Module:5	**Two-Port Networks and Network Graphs**	**7 hours**
Two-Port Networks-Impedance Parameters, Admittance Parameters, Hybrid Parameters, Transmission Parameters, Relationships Between Parameters, and Interconnection of Networks. Network Graphs-Incidence, Tie-Set, and Cut-Set Matrices for Circuit Analysis.		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
Charles K. Alexander, Matthew N. O. Sadiku, "**Fundamentals of Electric Circuits**", McGraw-Hill Higher Education, United States, 7th Edition, **2020** Abhijit Chakrabarti, "**Circuit Theory Analysis and Synthesis**", Dhanpat Rai & Co., India, 7th Edition, **2018**		
Reference Books		
A. Sudhakar, Shyammohan S. Palli, "**Circuits and Networks: Analysis and Synthesis**", McGraw-Hill, India, 5th Edition, **2017** M. E. Van Valkenburg, T.S. Rathore, "**Network Analysis**", Pearson Education, England, 3rd Edition, **2019** Mahmood Nahvi, Joseph A. Edminister, "**Schaum's Outline of Electric Circuits**", McGraw-Hill Education, United States, 7th Edition, **2018** W.H.Hayt, J.E.Kemmerly & S.M.Durbin, "**Engineering Circuit Analysis**", McGraw-Hill Higher Education, United States, 9th Edition, **2019**		
Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test		
Recommended by Board of Studies :	23-05-2025	
Approved by Academic Council : No. 78	12-06-2025	

Course Code	Course Title	L	T	P	C
BAECE202	Engineering Electromagnetics	3	1	0	4
Pre-requisite	Nil	Syllabus Version			
		1			

Course Objectives

1. Introduce the basic concepts of Electrostatics & Magnetostatics
2. Study the propagation of EM wave in different conducting and dielectric media through time varying Maxwell's equations.
3. Familiarize the concept of transmission lines and design of matching circuits

Course Outcomes

1. Compute Electrostatic fields & magneto static fields using theorems and laws
2. Interpret time varying fields and propagation of EM wave in different media.
3. Compute the parameters of transmission lines
4. Illustrate Impedance matching circuits using Smith chart
5. Interpret wave propagation mechanisms and radiation characteristics of various antennas using electromagnetic concepts.

Module:1	Introduction to Electromagnetics	17 hours

Coordinate systems, Divergence, Gradient and Curl. Coulomb's Law, Electric Fields due to Different Charge distributions, Gauss Law and Applications, Electrostatic Potential, Potential Gradient, Electric Dipole, Polarization in Dielectrics, Boundary conditions, current density, Convection, and conduction current densities continuity equation. Biot-Savart's Law, Ampere's Circuit Law and Applications, Magnetic Flux Density, Magnetic Scalar and Vector Potentials, Boundary conditions.

Module:2	Time Varying Fields	9 hours

Faraday's Law and Lenz law, Maxwell's Equations in Integral and differential form, Wave equation, Uniform plane wave propagation in lossy dielectrics, Lossless Dielectrics, Good Conductors and free space. Polarization, Power, and Poynting Vector.

Module:3	Transmission Lines	10 hours

Types, Parameters, Transmission Line Equations, Primary & Secondary Constants, Expressions for Characteristic Impedance, Propagation Constant, Phase velocity, input impedance, Reflection Coefficient, VSWR. Characterization of lossless, low loss and distortionless transmission lines. Significance of short circuit and open circuit lines of length λ/8, λ/4 and λ/2. Coaxial line, Planar transmission lines –Types, Microstrip Lines: field distribution, design equations, Q factor, losses in microstrip lines (qualitative). Basics of EMI/EMC(Qualitative)

Module:4	Smith Chart and Matching Circuits	12 hours

Smith Chart configuration and applications: Input impedance, admittance, VSWR, Reflection Coefficient, return loss, standing wave pattern. Matching Circuit Design- Quarter wave, Impedance Transformer, Single Stub and Lumped element matching.		
Module:5	**Waveguides and Radiation principles**	**10 hours**
TEM, TE and TM waves, Parallel plate waveguide, Rectangular waveguide, Characteristics of wave guides. Circular waveguide (Qualitative study). Radiation fundamentals, antenna parameters (radiation pattern, gain, bandwidth), different types of antennas a dipole, loop, and patch (Qualitative study)		
Module:6	**Contemporary Issues**	**2 hours**
Industry Expert Guest Lectures		
	Total Lecture Hours:	**60 hours**
	Tutorial Hours:	**15 hours**

Text Book(s)

William Hayt and John Buck, "**Engineering Electromagnetics**", Tata McGraw Hill , 8th Edition, **2017**
D. M. Pozar, "**Microwave engineering**", Wiley and Sons, 5th Edition, **2024**

Reference Books

Mathew O. Sadiku, "**Elements of Electromagnetics**", Oxford University Press, 7th Edition, **2021**
E.C. Jordan and K.G. Balmain, "**Electromagnetic Waves and Radiating Systems**", PHI, 2nd Edition, **2015**
David K Cheng, "**Fundamentals of Engineering Electromagnetics**", Pearson, 2nd Edition, **2014**
David J Griffiths, "**Introduction to Electrodynamics**", Pearson, 4th Edition, **2017**

Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test

Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAECE204	Microcontroller and Embedded C Programming	3	0	2	4
Pre-requisite	BAECE102/BAEVD102	Syllabus Version			
		1			

Course Objectives

1. Describe the architecture of 8051 and ARM-based microcontroller - LPC 2148.
2. Familiarize learners with the instruction sets of the ARM 7 processor and Embedded C programming of 8051 and LPC 2148 microcontrollers.
3. Familiarize interface peripherals with the microcontrollers to solve real-life problems.

Course Outcomes

1. Interpret the concepts of C programming in microcontroller applications.
2. Illustrate the architecture and programming structures of the 8051 microcontroller.
3. Employ the I/O interfacing concepts of the 8051 microcontroller using Embedded C programming.
4. Implement ARM architecture concepts using ARM assembly and C programming.
5. Develop embedded C programs for microcontroller-based applications.

Module:1	Overview of C programming	10 hours

Comments, identifiers, variables, headers, data types, operators, order of operators, format specifiers, escape sequence characters, input and output statements, programs on sequential statements. Control statements: if, if-else, switch, Loops: do-while, while, for loops and nested loops, Break, continue, goto and exit statements, Arrays: one-dimensional and two-dimensional array, Programs on arrays, strings, functions.

Module:2	8051 Architecture and Programming	12 hours

Introduction to Microprocessor and Microcontroller, 8051 Microcontroller: Architecture, Pin details, Memory organization, 8051 Embedded C programming: data types, Time delay generation, Arithmetic and Logical operations, data conversion programming, accessing code ROM space, data serialization, 8051 peripheral programming: I/O programming, Timer, counters, Interrupts, Serial Communication.

Module:3	I/O Interfacing with 8051 and its programming in Embedded C	6 hours

7-Segment LED display, LCD and Keyboard Interfacing, ADC with Sensor interfacing, DAC with actuator interfacing.

Module:4	ARM architecture	4 hours

Comparison between CISC and RISC, ARM Design Philosophy; Overview of 32-bit ARM-7 architecture; States - ARM, Thumb, Jazelle; Registers, Program status register; Processor Modes; Pipelining; Vector Tables; Exception handling.		
Module:5	**ARM Programming**	**11 hours**
ARM-7 Instructions - Data transfer instructions; Arithmetic and Logical instructions; Multiply instructions; Branches and subroutines; Load/Store instructions; Swap instruction; Pre and Post Indexing; Loading constants, SWI instruction, Conditional Execution; Assembly programming of ARM. ARM Core based Microcontroller and its programming in C language**-** Architecture of LPC2148, I/O ports, Timers/counter.		
Module:6	**Contemporary Issues**	**2 hours**
Industry Expert Guest Lectures		
	Total Lecture Hours:	**45 hours**

Text Book(s)

Mohammad Ali Mazidi, Janice G. Mazidi, Rolin D. McKinlay, "**The 8051 Microcontroller and Embedded Systems**", Pearson, 2nd Edition, **2014**

Andrew N.Sloss, Dominic Symes, Chris Wright, "**ARM system Developer's Guide**", Techno series, 1st Edition, **2024**

Reference Books

Mike McGrath, "**C programming in easy steps**", In Easy steps Limited, 4th Edition, **2019**

Muhammad Ali Mazidi, "**ARM Assembly Language Programming & Architecture**", MicroDigitaled, 2nd Edition, **2016**

NXP Semiconductors, "**LPC2148 User manual**", NXP Semiconductors, 4th Edition, **2014**

Steve Furber, "**ARM system On Chip Architecture**", Pearson Education, 2nd Edition, **2015**

Kenneth Ayala, "**The 8051 Microcontroller & Embedded Systems Using Assembly and C**", Cengage Learning, 1st Edition, **2010**

Indicative Experiments

1. Arithmetic and logical operations using Embedded C Programming of 8051	2 hours
2. Data conversion using Embedded C Programming of 8051	2 hours
3. Programming of I/O ports using Embedded C for 8051	2 hours
4. Programming of timers using Embedded C for 8051	2 hours
5. Programming of serial ports using Embedded C for 8051	2 hours
6. Programming of timer interrupt and serial interrupt using Embedded C for 8051	2 hours

7. LCD interfacing with 8051	2 hours
8. Keypad interfacing with 8051	2 hours
9. ADC /DAC interfacing with 8051	2 hours
10. ARM assembly programming- arithmetic and logical operations	2 hours
11. ARM assembly programming- data transfer instructions	2 hours
12. ARM assembly programming - branch and subroutines	2 hours
13. Embedded C Programming GPIO pins of ARM – based microcontroller LPC2148	2 hours
14. Generation of delay using timers of ARM –based microcontroller LPC2148	2 hours
15. Interfacing of seven segment display with ARM –based microcontroller LPC2148	2 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment	
Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAECE205	Control Systems	3	1	0	4
Pre-requisite	Nil	Syllabus Version			
		1			

Course Objectives

1. Analyze the performance of control systems in the time and frequency domains.
2. Design the controllers and compensators using frequency domain method
3. Analyze the behavior of systems utilizing state space model and AI/ ML

Course Outcomes

1. Examine various types of systems, mathematical models, feedback principles, and examples across different domains, including electrical and mechanical systems
2. Determine the transient and steady-state responses of control systems
3. Analyze system stability using Routh-Hurwitz criterion, root locus techniques and pole-zero placements
4. Analyze frequency response characteristics, controllers and compensators design using Bode plot, Nyquist plot, gain margin, and phase margin for system stability
5. Analyze the dynamics of control systems using state-space model and AI/ ML

Module:1	Introduction to Control Systems	9 hours

Types of Systems: Open-loop and Closed-loop Systems, Effects of Feedback on System Parameters, Mathematical Modelling, Transfer Functions, Block Diagrams, Signal Flow Graphs, Examples of Control Systems: Electrical and Mechanical Systems

Module:2	Time Domain Analysis	9 hours

Standard Test Signals: Step, Ramp, Impulse, and Parabolic Inputs, Time Response Analysis: First and Second Order Systems, Transient and Steady-State Responses: Damping Ratio, Natural Frequency, Rise Time, Settling Time and Peak Overshoot, Error Analysis: Steady-State Error and Error Constants

Module:3	Stability Analysis	7 hours

Concept of Stability: Absolute, Relative, Marginal Stability, Stability Criteria: Routh-Hurwitz Criterion and Root Locus Techniques, Effect of Addition of Poles and Zeros.

Module:4	Frequency Domain Analysis	9 hours

Frequency Response: Bode Plot, Nyquist Plot, and Gain/ Phase Margins, Stability in Frequency Domain, Controller Design using Frequency Domain: PD, PI, PID Controllers, Lead/ Lag Compensators.

Module:5	State-Space Analysis and Intelligent Control Systems	9 hours

Introduction to Modern Control Systems, State Variables, State and Output Equations, Controllability and Observability, Discrete-Time Systems, System Time Response, Characteristics - Jury‘s Stability Test, AI/ ML in Intelligent Control Systems.		
Module:6	**Contemporary Issues**	**2 hours**
Industry Expert Guest Lecture		
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
Norman S. Nise, "**Control Systems Engineering 2019**", Wiley, 8th Edition, **2019** Katsuhiko Ogata, "**Modern Control Engineering**", Prentice Hall, 5th Edition, **2010**		
Reference Books		
Benjamin C. Kuo, "**Automatic Control Systems**", Wiley, 9th Edition, **2013** Richard C. Dorf and Robert H. Bishop, "**Modern Control Systems**", Pearson, 12th Edition, **2011** Franklin, Gene F.; Powell, J. Da; Emami-Naeini, Abbas, "**Feedback Control of Dynamic Systems**", Pearson., 8th Edition, **2020**		
Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Seminar, Presentation		
Recommended by Board of Studies :	23-05-2025	
Approved by Academic Council : No. 78	12-06-2025	

Course Code	Course Title	L	T	P	C
BAEVD101	Electronic Devices	3	0	2	4
Pre-requisite	BAPHY108 Semiconductor Physics	Syllabus Version			
		1			

Course Objectives

1. Apply the semiconductor fundamentals and physics to electronic and optoelectronic devices
2. Equip students with the basics of semiconductor devices and their functions, culminating in the state-of-the-art device design and circuit application for future electronics
3. Perform experiments and optionally simulations associated with the theory on device characteristics and apply the knowledge in various electronic circuits

Course Outcomes

1. Employ the semiconductor fundamentals to homo- and hetero-semiconductor junctions and electronic devices
2. Evaluate the bipolar junction transistor and FET parameters in different configurations for electronic circuits
3. Use the work function difference and energy band diagram concepts to the MOS capacitor
4. Compute the MOSFET threshold voltage and characteristics
5. Employ simulation tools and hardware studies of the electronic devices and circuits

Module:1	Semiconductor Fundamentals	6 hours

Direct and indirect band gap, Density of states, Fermi-Dirac distribution, Fermi level, Intrinsic and extrinsic semiconductors, Equilibrium carrier concentration, Concept of Equilibrium, Non equilibrium and Steady state, Excess Carriers, Electron-hole pair creation by radiation, Carrier lifetime, Quasi equilibrium and quasi-Fermi level. Generation and recombination of carriers - Excess carrier Lifetime, Semiconductor in the electric field. Carrier drift, Mobility and velocity saturation, Carrier diffusion, Einstein's relation, Poisson equation, Continuity equation.

Module:2	PN Junctions and Metal Semiconductor Junctions	12 hours

PN Junction – Thermal Equilibrium Energy band diagram - Contact potential and space charge layers -Poisson equation - Electric fields and Potentials, PN junction under applied bias - Energy band diagrams - One-sided PN junction – Avalanche and Zener breakdown, Zener diode. Diode capacitances, small signal model of PN junction, Static current-voltage characteristics of PN junctions, Metal-Semiconductor Contacts: Schottky, and Ohmic contacts, Linearly Graded Junction, Non-ideal junctions, Heterojunctions. Solar Cells.

Module:3	Bipolar Junction Transistors	7 hours

Bipolar Junction Transistors: Device structure and physical operation, current-voltage relationship - Common Base- common base current gain (α), Common Emitter configurations – Base width modulation (Early effect)-current emitter current gain (β); small signal and equivalent circuit models. High-level injection effects -Current crowding.		
Module:4	**MOS Capacitor**	**8 hours**
MOS Capacitor: Ideal and realistic MOS Capacitors, Contact potential – Gate work function, Energy-band diagrams, Flat-band condition, Oxide and Interface charges, Accumulation, Depletion, Inversion, Strong inversion, Threshold voltage calculation, Body effect, Capacitance voltage characteristics.		
Module:5	**Field Effect Transistors**	**10 hours**
JFETs: Construction, Operation, and Characteristics. MOSFETs: MOSFET Physics, Surface Mobility, Drain current, Saturation voltage, Current-voltage characteristics, leakage currents, Short channel effects - Velocity saturation, Channel length modulation, Sub-threshold conduction - Vt roll-off, Drain-induced barrier lowering, Punch-through - Hot carrier degradation, Gate induced drain leakage, Gate leakage, MOSFET small signal model.		
Module:6	**Contemporary issues**	**2 hours**
	Total Lecture Hours:	**45 hours**

Text Book(s)

Donald A. Neamen, "**Semiconductor Physics and Devices- Basic Principles**", McGraw Hill, 4th Edition, **2021**
B. G. Streetman and S. Banerjee, "**Solid State Electronic Devices**", PHI Private Limited, 7th Edition, **2015**

Reference Books

Pallab Bhattacharya, "**Semiconductor Optoelectronic Devices**", Prentice Hall of India Pvt Ltd, **2006**
Robert F Pierret, "**Semiconductor Device Fundamentals**", Pearson Education, **2006**
S. M. Sze and Kwok K. Ng, "**Physics of Semiconductor Devices**", John Wiley and Sons, **2007**
P. Chakrabarti, "**Optoelectronic Devices and Optical Fiber Communication**", CBS Publishers and Distributors Pvt Ltd, **2024**
M.S Tyagi, " **Introduction to Semiconductor Materials and devices**", John Wiley and Sons, 5th Edition, **2005**
B. Jayant Baliga, "**Fundamentals of Power Semiconductor Devices**", Springer, 2nd Edition, **2019**

Indicative Experiments

1. Measure the I-V characteristics of PN Junction Diode and Zener Diode:	6 hours

(i) Simulation of I-V characteristics of PN Junction Diode and Zener Diode. (ii) Simulation of I-V characteristics and Energy band diagram of PN Junction Diode using TCAD	
2. Diode Applications: Half Wave and Full Wave Rectifier without Filter and with Filters.	4 hours
3. Zener Diode Applications: Design of Zener Diode Regulator: (i) Line regulation (ii) Load Regulation	4 hours
4. BJT: (i) Input and Output Characteristics of CB and CE configurations. (ii) BJT biasing circuits and fixing operating point.	6 hours
5. FET: (i)JFET (NFET and PFET)Transfer and Output Characteristics. (i) MOSFET (NMOS and PMOS) Transfer and Output Characteristics. (iii) Design of CMOS inverter and simulation of Voltage Transfer Characteristics (VTC) and Transient Characteristics of CMOS inverter	6 hours
6. Design of MOSFET-based CS Amplifier and simulate the transient response and Frequency response of CS Amplifier.	4 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment, Oral Examination	
Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD102	Digital System Design	3	0	2	4
Pre-requisite	NIL	Syllabus Version			
		1			

Course Objectives

1. Introduce the fundamentals of Boolean algebra and digital logic design.
2. Equip students with design and HDL coding skills for combinational and sequential circuit implementation.
3. Prepare students to the concept of finite state machine for solving sequential logic problems on programmable devices.

Course Outcomes

1. Apply the knowledge of Boolean algebra and Karnaugh-maps to optimize the digital logic.
2. Implement the various combinational and sequential circuits for customized specification.
3. Utilize the Verilog HDL constructs to model all the combinational and sequential logic circuits.
4. Apply FSM concepts to construct state transition diagrams and state tables for given sequential logic problems.
5. Interpret various PLD/FPGA/SOC architectures and implement the digital circuits on programmable devices.

Module:1	Boolean algebra	8 hours

Basic definitions, Basic postulates and theorems, Properties of Boolean Algebra, Canonical (SOP and POS Forms), Logic minimization, Karnaugh-maps, NAND and NOR realization and Representation of Boolean expression in static CMOS logic style

Module:2	Verilog HDL	7 hours

Lexical Conventions, Ports and Modules, Operators, Dataflow Modeling, Gate Level Modelling, Behavioural Modeling, Tasks and functions,Test Bench, Synthesiable coding Style.

Module:3	Design and Modeling of combinational logic circuits	10 hours

Half Adder, Full Adder, Half Subtractor, Full Subtractor, Encoder, Decoders, Multiplexers, De-multiplexers, Parity generator and checker, Realization of digital circuits using Decoder, Multiplexer and De-multiplexer. Datapath circuits - N-bit Parallel Adder/Subtractor, Carry Look Ahead Adder, Unsigned Array Multiplier, Booth Multiplier, Magnitude comparator. Design and Modeling of Combinational and Datapath circuits.

Module:4	**Design and Modeling of Sequential logic circuits**	**10 hours**
Latches and flip-flops - SR-latch, D-latch, D flip-flop, JK flip-flop, T flip-flop, Setup and Hold parameters, Static and Dynamic hazards; race free design; Shift Registers - SISO, SIPO, PISO, PIPO, Universal shift register, Design of synchronous counters - Up, Down, UP/Down, Modulo-n, Ring, Johnson, Counters for random sequence using D, T, and JK flip flops, and Asynchronous counters; Design and Modeling of Sequential logic circuits.		
Module:5	**Finite state machine and FPGA Overview**	**8 hours**
Design and modelling of Finite State Machine - Moore and Mealy state machines; State machine as a sequence detector, serial adder, vending machine; Subsystem design – ALU, FIFO; FPGA - Programming Technologies-Chip I/O- Programmable Logic Blocks- Fabric and Architecture of FPGA .		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**

Text Book(s)

M. Morris Mano and Michael D. Ciletti, "**Digital Design: With an Introduction to the Verilog HDL and System Verilog** ", Pearson Pvt. Ltd., 6th Edition, **2018**
Vaibbhav Taraate, "**Digital Logic Design Using Verilog Coding and RTL Synthesis** ", Springer, 2nd Edition, **2022**

Reference Books

Ming-Bo Lin, "**Digital Systems Design and Practice: Using Verilog HDL and FPGAs,** ", Create Space Independent Publishing Platform , 2nd Edition, **2015**
J. Bhasker, "**A Verilog HDL Primer,** ", Star Galaxy Publishing , 3rd Edition, **2018**

Indicative Experiments

1. Modeling of Universal and Basic Gates	2 hours
2. Simplify the Boolean expression and model them	2 hours
3. Design and model the data path elements – Adders / Subtractors	2 hours
4. Implementation of data path elements on FPGA platform	4 hours
5. Design and model the combinational circuits	2 hours
6. Implementation of combinational circuits on FPGA platform	4 hours
7. Design and model the sequential circuits – Flipflops, counter	2 hours
8. Implementation of sequential circuits on FPGA platform	4 hours

9. Design and model the FSM based design – Serial Adder, vending machine, traffic light controller	4 hours
10. Implement of complex design on FPGA – ALU, FIFO	4 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test	
Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD201	**Electronic Circuits**	**3**	**0**	**2**	**4**
Pre-requisite	BAEVD101 Electronic Devices	**Syllabus Version**			
		1			

Course Objectives

1. Describe the fundamental principles underlying design of various building blocks and amplifier circuits using Bipolar Junction Transistors and analyze their performance characteristics.
2. Understand op-amp performance characteristics and its applications.
3. Understand waveform generators and oscillators.

Course Outcomes

1. Illustrate the various building blocks of Electronic Circuits such as Diodes, Rectifiers, BJT Current Mirrors, BJT Amplifiers and their characteristics.
2. Apply Multistage Configurations and Feedback Techniques in Amplifier Design.
3. Interpret the fundamentals of op-amp and its various configurations.
4. Implement op-amp based circuits to generate various waveforms and oscillators.
5. Interpret the behavior of Electronic Circuits using breadboard / SPICE software.

Module:1	**Basic Building Blocks of Electronic Circuits**	**9 hours**

DC and AC Analysis of Diodes, Applications of Diode- Rectifiers, Clippers, Clampers
BJT- Current Sources, Current Mirrors, Darlington Configuration, DC and AC Analysis-Low and High Frequency Models- Common-Emitter, Common-Base, Common-Collector.

Module:2	**BJT Differential and Power Amplifiers**	**9 hours**

BJT Differential Pair, Large/Small Signal Models, Non-ideal characteristics, Differential Amplifier with Resistive Load, Active Load, Performance parameters of Differential amplifiers, Power Amplifiers-Class A, Class B, Class AB.

Module:3	**Multistage and Feedback Amplifiers**	**9 hours**

Multistage Amplifiers- AC Analysis of Cascade and Cascode Amplifiers, Stability analysis of multi stage amplifiers, Feedback Amplifiers-General Feedback Structure, Properties of Negative Feedback, Determination of loop gain, Various Feedback Topologies- Voltage Series, Voltage Shunt, Current Series, Current Shunt.

Module:4	**Operational Amplifiers and Comparators**	**9 hours**

Operational Amplifier as a Black Box-General Considerations and Op-Amp-Based Circuits Inverting, Non-Inverting, Difference Amplifier, Differentiator, Integrator,

Bipolar OpAmp- 741 internal Circuitry, DC/AC Analysis, Performance parameters of OpAmp, Instrumentation Amplifiers, Comparators and Schmitt trigger.		
Module:5	**Waveform generators and Oscillators**	**7 hours**
Waveform generators- Square Wave and Triangular Waves, Rectifier, Peak Detectors. Basic Principles of Oscillators, Op-Amp RC Oscillators- Phase Shift, Wein's Bridge. 555 timer- Astable and Monostable Multivibrators, and its applications		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**

Text Book(s)

Adel.S.Sedra & Kenneth C. Smith, Tony Carusone, Vincent Gaudet, "**Microelectronics Circuits**", Oxford University Press, New York, 8th Edition, **2021**
D Roy Choudhury, Shail B Jain, "**Linear Integrated Circuits**", New Age International India, 6th Edition, **2021**

Reference Books

Behzaad Razavi, "**Fundamentals of Microelectronics**", Wiley Publications, Hoboken, New Jersey, 3rd Edition, **2021**
Donald A.Neamann, "**Microelectronics: Circuit Analysis & Design**", Mcgraw Hill, New York, 4th Edition, **2021**
Albert P. Malvino, David J. Bates, Patrick E. Hoppe, "**Electronic Principles**", McGraw Hill, Glencoe, 9th Edition, **2021**
Ramakant A. Gayakwad, "**Op-Amps and Linear Integrated Circuits**", Pearson Education, India, 4th Edition, **2015**

Indicative Experiments

1. Study of Diode Rectifier Circuits	2 hours
2. Study of Clipper and Clamper Circuits	2 hours
3. Study of Input/Output Characteristics of CE configuration.	2 hours
4. Study of Input/Output Characteristics of BJT Power Amplifiers- Class A, B, AB.	2 hours
5. Study of Characteristics of an NPN/PNP BJT based Differential Amplifier.	2 hours
6. Study of characteristics of an op-amp	2 hours
7. Op-amp as an Inverting and Non-Inverting Amplifier.	4 hours
8. Voltage/Current Feedback amplifier using op-amp	2 hours
9. Op-amp as an Integrator and Differentiator Amplifier	4 hours

10. Op-amp as a Comparator and Schmitt Trigger	4 hours
11. Op-amp as a Waveform Generator- Square Wave, Triangular etc. (Multivibrators)	2 hours
12. Oscillator design using op-amp -Wein's Bridge, RC Phase Shift	2 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment	
Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD202	**Computer Architecture**	**3**	**1**	**0**	**4**
Pre-requisite	BAEVD102 Digital System Design	**Syllabus Version**			
		1			

Course Objectives

1. Explain the fundamental and advanced computer architecture.
2. Impart the memory hierarchy and solutions to multi-processor architecture.
3. Introduce specialized and emerging architectures for AI/ML applications.

Course Outcomes

1. Interpret the fundamentals of general computer architecture and its performance.
2. Interpret between superscalar, VLIW and recent architecture.
3. Illustrate the memory hierarchy used in the single-core architectures.
4. Implement solutions for problems in parallel and distributed computing.
5. Employ the specialized and emerging architectures for AI/ML applications.

Module:1	**Fundamentals of Computer Architecture**	**9 hours**

Review of Basic Computer Architecture, Performance Metrics (CPI, IPC, Speedup, Amdahl's Law), Instruction Set Architecture (ISA), Pipelining: Hazards (Data, Control, Structural) & Solutions

Module:2	**Memory Hierarchy and Optimization**	**9 hours**

Cache Design: Associativity, Replacement Policies; Multi-level Caching, Victim Cache, Inclusive/Exclusive Cache; Virtual Memory, TLBs, and Page Table Optimization; Non-volatile memories (NVM), 3D-stacked Memory.

Module:3	**High Performance Processor Architectures**	**9 hours**

Superscalar and VLIW Architectures, Out-of-Order Execution & Register Renaming, Branch Prediction Techniques, SIMD and GPU Architectures, Recent Trends: RISC-V, ARM, and AI Accelerators

Module:4	**Parallel and Distributed Computing**	**8 hours**

Shared Memory Multiprocessing (SMP), Cache Coherence Protocols; Multi-core and Many-core Architectures; Distributed Systems, Cluster, and Cloud Computing; Interconnection Networks and Routing Techniques

Module:5	**Emerging and Specialized Architectures**	**8 hours**

Reconfigurable Computing (FPGA, CGRA); Neuromorphic and Quantum Computing; Domain-Specific Architectures (TPUs, Edge AI Processors); Security in Modern Architectures (Spectre, Meltdown, RISC-V Security)

Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**

Text Book(s)

John L. Hennessy , David A. Patterson, "**Computer Architecture: A Quantitative Approach**", Morgan Kaufmann, 7th Edition, **2025**
Jim Ledin, Dave Farley, "**Modern Computer Architecture and Organization**", Packt Publishing, 2nd Edition, **2022**

Reference Books

Andrew S. Tanenbaum, "**Structured Computer Organisation**", Pearson Education, 5th Edition, **2006**
William Stallings, "**Computer organization and architecture: designing for performance**", Pearson Education India, 11th Edition, **2019**
Carl Hamacher, Zvonko Vranesic and Safwat Zaky, "**Computer Organization**", McGraw Hill Education, 5th Edition, **2011**

Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test

Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD203	Communication Systems	3	1	0	4
Pre-requisite	NIL	Syllabus Version			
		1			

Course Objectives

1. Enrich students with the basics of communication systems and mathematical modelling of amplitude and angle modulation schemes.
2. Provide in-depth knowledge of sampling, quantization, waveform coding techniques and digital modulation schemes for modern communication systems.
3. Introduce the theoretical foundations of information theory and various encoding techniques for reliable data transmission.

Course Outcomes

1. Illustrate the process of amplitude modulation and demodulation using time and frequency domain representations
2. Interpret the generation and detection of angle modulation schemes and performance improvement methods.
3. Apply waveform coding techniques to represent and reconstruct digital signals.
4. Apply mathematical concepts to represent digital modulation schemes and their Bit Error Rate.
5. Apply concepts of information theory and encoding techniques to enhance data transmission.

Module:1	Amplitude Modulation	5 hours

Block diagram of communication system, Need for modulation, Amplitude Modulation – AM, DSBSC, SSB,VSB methods of modulation and demodulation, Super heterodyne receivers

Module:2	Angle Modulation	6 hours

Basic concepts of Phase Modulation, Frequency Modulation, types of FM, Generation of FM Signal- Armstrong Method, Detection of FM Signal- Balanced slope detector, Phase locked loop, Comparison of FM and AM., Concept of Pre-emphasis and de-emphasis.

Module:3	Waveform Coding Techniques	10 hours

Waveform coding techniques - Pulse Code Modulation (PCM), Differential Pulse Code Modulation (DPCM), Delta Modulation (DM), Representation of Line Codes– Unipolar, Polar, Bipolar using NRZ and RZ, Manchester format.

Module:4	Digital Modulation Techniques	11 hours

Gram-Schmidt Orthogonalization Procedure. Correlation and Matched filter receiver - modulation and demodulation techniques - BASK, BPSK, BFSK, QPSK: BER with AWGN and Bandwidth efficiency analysis.

Module:5	Principles of Information Theory	11 hours

Uncertainty, self-information, average information, mutual information and channel capacity, Shannon Harley law, Source coding theorem, Huffman coding, Error correcting codes- Linear block codes: encoder design, syndrome calculator circuit, decoder design. Convolutional Codes- Code tree, State diagram.		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**

Text Book(s)

Simon Haykin, "**Communication Systems**", Wiley India, 5th Edition, **2021**
B. P. Lathi & Zhi Ding, "**Modern Digital and Analog Communication Systems** ", Ozford University Press India, 5th Edition, **2022**

Reference Books

Bernard Sklar and Fredric J. Harris , "**Digital Communications — Fundamentals and applications** ", Pearson, 3rd Edition, **2020**
Simon Haykin and Michael Moher, "**Introduction to Analog and Digital Communication**", Wiley India, 2nd Edition, **2019**
K.Sam Shanmugam , "**Digital and Analog Communication Systems**", Wiley, 1st Edition, **2012**

Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test

Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD204	Signal Processing	3	0	2	4
Pre-requisite	NIL	Syllabus Version			
		1			

Course Objectives

1. Provide a foundational understanding of signals and systems for analyzing and designing various systems and applications
2. Introduce signals and systems in both the time and frequency domains, using techniques like Fourier series, Fourier transforms, and Laplace & Z-transforms
3. Enable the design and realization of digital IIR and FIR filters using transformation techniques, windowing methods, and filter structures for practical signal processing applications.

Course Outcomes

1. Interpret the mathematical representation of signals and systems, including signal operations, system classification and analysis
2. Apply Fourier, Laplace, and Z-transforms to analyse signals and systems in various domains
3. Implement digital IIR and FIR filters using transformation, windowing techniques and realize the structures for signal processing applications
4. Compute the impact of finite word length on the performance of DSP systems, including quantization effects and limitations of fixed-point DSP.
5. Interpret signal processing techniques and digital filters using both simulation and hardware platforms

Module:1	Signals and Systems	9 hours

Introduction to Signals: Classification of signals-continuous and discrete, Operations on CT and DT signals: time and amplitude scaling, shifting, arithmetic operations, Sampling- Nyquist rate. Introduction to Systems: System classification: Linear, Time varying/invariant, causal, BIBO stable, static/dynamic, Discrete time convolution and correlation.

Module:2	Frequency Domain System Analysis	12 hours

Frequency Domain Analysis-I: Introduction to Fourier Series, Continuous-time Fourier transform, Discrete-time Fourier transform - Dirichlet's Conditions, Gibbs Phenomenon. Magnitude and phase response, Properties, system analysis. Frequency Domain Analysis-II: Introduction to Laplace Transform- Solution to differential
equations, Z-transform, Properties, S-plane to Z-plane mapping, Inverse z-transform, Solution to difference equations using z-transform, Region of convergence, stability analysis, DFT-circular convolution, Radix-2 FFT Algorithms – Decimation In Time-FFT.

Module:3	Design of Filters	9 hours

Digital IIR filters: Design of Digital IIR Butterworth and Chebyshev Type–I Filter from the given analog transfer function H(s) -pre-warping- Bilinear Transformation Techniques. Design of FIR filters: Linear phase FIR filters, Design of Digital FIR Filters with windowing method -Rectangular, Bartlett, Hamming, Hanning and Blackman, Frequency Sampling techniques		
Module:4	**Realization of Digital Filters**	**6 hours**
Basic FIR and IIR digital filter structures - Direct Forms-I & II, Cascade, Parallel, Lattice and Lattice-Ladder structures- All pass filters.		
Module:5	**Digital Signal Processors**	**7 hours**
Programmable Digital Signal Processors: Introduction, Evolution of Programmable Digital Signal Processors, Features of DSP Processors. Fixed-point Architecture - VLIW, Fixed- point and Floating-point coefficients, introduction to finite word length effects.		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**

Text Book(s)

John G. Proakis, Dimitris G Manolakis, "**Digital Signal Processing: Principles, Algorithms and Applications,**", Pearson USA, 5th Edition, **2022**

A.V. Oppenheim, A.S. Willsky & S.H. Nawab,, "**Signals & Systems,** ", PHI, 2nd Edition, **2004**

Reference Books

S. K. Mitra, "**Digital Signal Processing: A Computer based Approach**", McGraw Hill, 4th Edition, **2013**

P. P. Vaidyanathan, "**Signals, Systems, and Signal Processing.**", Cambridge University Press, 1st Edition, **2024**

Simon Haykin, Barry Van Veen, "**Signals and Systems**", Wiley Publications, 2nd Edition, **2021**

B.P. Lathi and Roger Green, "**Linear Systems and Signals**", Oxford University Press, 3rd Edition, **2020**

R. Keshab K. Parhi, "**VLSI Digital Signal Processing Systems, Design and implementation** ", Wiley Interscience, 2nd Edition, **2007**

Indicative Experiments

1. Generation of elementary continuous time (CT) and Discrete time (DT) signals	4 hours
2. Operation on DT Signals	4 hours
3. LTI System Analysis in time domain: Convolution and Correlation	4 hours

4. Frequency domain analysis of the signals and systems – ZT , DTFT and DFT, FFT.	6 hours
5. Signal processing in hardware	4 hours
6. Design of Digital filters: FIR and IIR	4 hours
7. Design of digital filters for processing biomedical/audio/speech signals.	4 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment	
Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD205	VLSI Circuit Design	3	0	2	4
Pre-requisite	BAEVD102 Digital System Design	Syllabus Version			
		1			

Course Objectives

1. Introduce the basic concepts and techniques of modern integrated circuit design.
2. Describe the fundamental principles underlying digital design using CMOS logic and analyze the performance characteristics of these digital circuits.
3. Verify that a design meets its functionality, timing constraints, both analytically and through computer-aided design tools.

Course Outcomes

1. Illustrate the stages of the VLSI design process, MOSFET characteristics, and the operation of CMOS inverters.
2. Demonstrate CMOS process technologies and the key layout design rules.
3. Interpret the DC transfer characteristics, power dissipation, CMOS logic families, sequential logic and timing analysis.
4. Demonstrate basic interconnects and memories.
5. Implement CMOS digital circuits, inverters, logic gates, memory cells, and arithmetic circuits.

Module:1	MOSFET Theory	9 hours

VLSI Design Flow, Device Structure, Electrical behavior of MOS transistors, Capacitance- Voltage Characteristics and Non-ideal Effects; Effects of scaling on MOSFETs. CMOS Inverter and complex logic gates.

Module:2	CMOS Layout Design	9 hours

CMOS Process Technologies: N-well, P-well, Latch-up in CMOS, Stick Diagram using Euler's Theorem, Layout Design Rules. Layouts of complex logic gates.

Module:3	CMOS Performance analysis	8 hours

MOS Inverter: DC Transfer Characteristics, Static and Dynamic Behavior, Delay Estimation, Logical Effort and Transistor Sizing, Static and Dynamic Power Dissipation.

Module:4	CMOS Combinational and Sequential Logic circuits	7 hours

CMOS Logic Families: Pass Transistor Logic, Transmission Gates, Pseudo NMOS, Cascode Voltage Switch Logic and dynamic logic. CMOS Sequential Logic circuits: Latches and Flip Flops, Dynamic Flip Flops, Setup Time, Hold Time calculation.

Module:5	Interconnects and Memories	10 hours

Interconnect Modeling: resistance, Capacitance, Interconnect Impact: Delay, crosstalk. Interconnect Engineering: Width, Spacing of layers and Repeaters. Introduction to Memory Systems, Read-Only Memory (ROM) Circuits, Static RAM (SRAM) Circuits, Dynamic RAM (DRAM) Circuits. Memory peripherals.		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**

Text Book(s)

Neil H.Weste, Harris, A. Banerjee, "**CMOS VLSI Design, A circuits and System Perspective**", Pearson Education, 4th Edition, **2015**

Jan M. Rabaey, Anantha Chadrakasan, Borivoje Nikolic, "**Digital Integrated Circuits: A Design Perspective**", Pearson Education, 2nd Edition, **2021**

Reference Books

Yu, Shimeng., "**Semiconductor Memory Devices and Circuits.**", CRC Press, 1st Edition, **2022**

Sung-Mo Kang, Yusuf Liblebici, Chulwoo Kim,, "**CMOS Digital Integrated Circuits: Analysis and Design**", Tata Mc Graw Hill, 4th Edition, **2019**

Indicative Experiments

1. Parameter extraction for basic cell structure (NMOS and PMOS devices). Analysis of MOS with width variation, body effect and estimation of channel length modulation	2 hours
2. Design Layout of CMOS logic circuits and perform post-layout simulation.	4 hours
3. Design and Analysis of CMOS inverter for arbitrary sizing. Estimation of Power, Delay, Noise Margin. Impact of load on performance metrics.	4 hours
4. Analysis of CMOS inverter for given specification	2 hours
5. Analysis of inverter chains using progressive sizing to improve delay performance	2 hours
6. Design and Analysis of Universal gates in static CMOS logic	2 hours
7. Design and Analysis of Combinational circuits (adder, decoder, mux, Barrel shifter)	2 hours
8. Design and Analysis of Pass transistor and Transmission gate-based circuits	4 hours

9. Design and Analysis of CMOS sequential circuits (Latches and Flip Flops) – Setup and hold time calculations.	4 hours
10. Design a CMOS Memory cell (SRAM, DRAM).	4 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment	
Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD301	Verification Methodologies	3	0	2	4
Pre-requisite	BAEVD102 Digital System Design	Syllabus Version			
		1			

Course Objectives

1. Understand the concepts of VLSI Verification Methodologies
2. Develop skills in writing testbenches using System Verilog
3. Apply industry standard framework for Verification

Course Outcomes

1. Interpret the basic test environment for verification
2. Implement system Verilog test environment
3. Implement reusable class based test environment
4. Interpret coverage metrics and improve verification efficiency
5. Employ industry-standard framework for verification

Module:1	Fundamentals of Verification	9 hours

Introduction to VLSI verification - Types of verification - Functional Verification challenges and solutions – Functional Verification Process - Verification planning – Basic Testbench Functionality – Layered Testbench - Directed Testing – Constrained Random Stimulus – Coverage – Code Coverage and Functional Coverage

Module:2	System Verilog	9 hours

Introduction to System Verilog – Literal values-data Types – Arrays – Array methods – Creating new types with typedef – user defined structures – Enumerated types – Packages – operators – expressions – Procedural statements and control flow – Processes in System Verilog – Task and functions – Routine arguments – Returning from a routine – SV scheduling semantics – Developing System Verilog Test environment – Case Study

Module:3	OOP based Testbench	8 hours

OOP Terminology - Creating Object - object deallocation - copying objects - static variables - Global variables – Inheritance – Polymorphism – Program – Interface - Stimulus timing - Module interactions (Mailbox, Semaphores) - Connecting together – Developing reusable object based self-checking test environment – Generator – Transactor – Driver - Monitor – Scoreboard – Case Study

Module:4	Randomization, Functional Coverage	8 hours

Need for Randomization – Randomization in System Verilog – Constraint Details – Solution Probabilities – Controlling Multiple Constraint Blocks – Valid Constraints – In-line Constraints – Common Randomization Problems - Coverage Types – Anatomy of covergroup – Triggering a covergroup – Data Sampling – Cross

Coverage – Coverage options – Developing constraint random verification environment		
Module:5	**Universal Verification Methodology (UVM) Basics**	**9 hours**
System Verilog test environment Vs UVM based test environment - Basics of UVM Transaction Level Communication Protocol - Developing reusable verification components - Developing reusable verification environment – Case Study		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**

Text Book(s)

Ashok B. Mehta, "**Introduction to System Verilog**", Springer, New York, 1st Edition, **2021**
Srivatsa Vasudevan, "**Practical UVM Step by Step with IEEE 1800.2**", R R Bowker, CA, USA, 2nd Edition, **2020**

Reference Books

Ashok B. Mehta, "**ASIC/SoC Functional Design Verification – A Comprehensive guide to Technologies and Methodologies**", Springer, New York, 1st Edition, **2017**
Christian B Spear, "**System Verilog for Verification: A guide to learning the Testbench language features**", Springer, 3rd Edition, **2012**

Indicative Experiments

1. Developing self-checking Verification Environment in Verilog	2 hours
2. Arrays in System Verilog	2 hours
3. Inheritance & Polymorphism	2 hours
4. Mailbox	2 hours
5. Developing reusable verification components	4 hours
6. Class based System Verilog self-checking test environment for FIFO	4 hours
7. Coverage	2 hours
8. UVM test environment	2 hours
9. UVM Components	4 hours
10. UVM testbench for APB/AHB Protocol	6 hours
Total Laboratory Hours:	**30 hours**

Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment	
Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD302	CMOS Analog IC Design	3	0	2	4
Pre-requisite	BAEVD201 Electronic Circuits	Syllabus Version			
		1			

Course Objectives

1. Develop the ability to design and analyze analog basic building blocks using MOSFET's.
2. Acquire the skills to design and analyze CMOS Analog Amplifiers.
3. Understand the architectures of Oscillators and PLL.

Course Outcomes

1. Illustrate the basic building blocks such as current sources, current mirror, reference circuits, single-stage amplifier with respect to frequency and noise.
2. Apply differential amplifier principles and feedback techniques in amplifier design.
3. Illustrate multistage amplifier with stability analysis
4. Demonstrate the fundamentals of oscillators and phase locked loop
5. Implement MOS amplifiers, according to design specifications in industry standard EDA tool.

Module:1	MOSFET Current Mirrors and Reference Circuits	9 hours

Overview of Analog Blocks in SoC Design, Review of MOS Device Physics- MOS Device models, MOS Current Sources and Sinks, Current Mirror- Basic Current Mirrors, Wilson Current Mirror, Cascode Current Mirrors, Threshold Reference Circuits.

Module:2	Basic CMOS amplifiers	9 hours

Common Source stage, Common Gate stage, Common Drain stage, Cascode stage, Miller effect, Frequency response of Common Source stage, Common Gate stage, Common Drain stage, Cascode stage, Noise in single stage amplifiers.

Module:3	CMOS Differential Amplifiers and Feedback Amplifiers	9 hours

Differential stage- Single-ended and Fully Differential operation, Basic Differential Pair- Frequency response of differential amplifier, Noise in differential amplifiers, Performance Parameters of Differential Amplifiers.
Feedback Amplifiers-Types of Feedback Amplifiers, Feedback configurations- voltage-voltage, current-voltage, current-current, voltage-current feedback.

Module:4	CMOS Operational Amplifiers	8 hours

General Considerations- Single, Multistage amplifiers- Frequency Response Analysis of Two Stage, Cascode, Gain Boosting, Common mode Feedback,

Performance Parameters of Operational Amplifiers-CMRR, ICMR, OCMR, PSRR, Slew Rate, Noise, Stability and Frequency Compensation of two stage Op-amp.		
Module:5	**Oscillators and PLL**	**8 hours**
Oscillators- General Considerations, Ring Oscillators, LC Oscillators, Voltage Controlled Oscillators. Phase Locked Loop- Basic PLL and its dynamics, Charge-pump PLL, Non-ideal Effects in PLL, PLL applications- Frequency Multiplier.		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**
Text Book(s)		
Behzad Razavi, " **Design of Analog CMOS Integrated Circuits**", McGraw-Hil, 2nd Edition, **2017** David Johns and Ken Martin, "**Analog Integrated Circuit Design**", John Wiley & Sons, Inc., 2nd Edition, **2012**		
Reference Books		
Phillip E. Allen and Douglas R. Holberg, "**CMOS Analog Circuit Design**", Oxford University Press, 2nd Edition, **2016**		
Indicative Experiments		
1. Plotting of C-V and I-V characteristics, gm vs. Vgs, Transit Frequency (fT)		2 hours
2. Analysis and Design of Simple Current Mirror and Cascode Current Mirror.		2 hours
3. Design of Single Stage Amplifiers- Common Source, Common Gate and Common Drain.		6 hours
4. Analysis and Design of Differential Amplifier with resistive load.		2 hours
5. Analysis and Design of Differential Amplifier with Active load and Current Source Load.		4 hours
6. Layout of differential amplifier and post-layout simulation		6 hours
7. Analysis and Design of Two-Stage op-amp with Frequency Compensation.		6 hours
8. Noise analysis of single stage amplifier.		2 hours
	Total Laboratory Hours:	**30 hours**
Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Final Assessment		
Recommended by Board of Studies :	23-05-2025	

Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD303	ASIC Design	3	0	2	4
Pre-requisite	BAEVD102 Digital System Design	Syllabus Version			
		1			

Course Objectives

1. Understand the fundamentals of ASIC design flow with respect to different cost functions
2. Recognize the importance of design for testability and static timing analysis in ASIC design
3. Comprehend the guidelines at each abstraction level in physical design and verification

Course Outcomes

1. Demonstrate ASIC design flow and the issues related to synthesis including technology choice, design environment and constraints
2. Apply testability techniques for test pattern generation and fault simulation tools to assess circuit reliability
3. Interpret the timing behavior of digital circuits using Static Timing Analysis techniques
4. Apply design rules, methods, and timing concepts to create efficient physical designs and resolve issues like congestion, IR drop, and electromigration
5. Utilize industry-standard EDA tools to implement, test and verify physical design stages

Module:1	RTL Synthesis	9 hours

Types of ASICs - Traditional and Physical Compiler based ASIC Flow - RTL synthesis Flow – Synthesis Design Environment & Constraints - Technology Library Basics– Components of Technology Library – Synthesis Optimization - Technology dependent synthesis - Formal Verification.

Module:2	Design for Testability	8 hours

Fault Models - Fault Simulation: Serial and parallel – Combinational ATPG : D-Algorithm - Design for Testability: Ad-Hoc Approach - Structured Approach - Scan Cell Designs - Scan Design Rules - Scan Design Flow – Logic BIST – Boundary scan architecture

Module:3	Static Timing Analysis	10 hours

Timing Parameter Definition – Setup Timing Check- Hold Timing Check - Setup and Hold Violation Fixing - Multicycle Paths - Half Cycle Paths - False Paths – Clock skew optimization – On-Chip Variations (OCV) – Advanced OCV - Time Borrowing

Module:4	Physical Design	9 hours

Physical Design Flow- Guidelines for Floor plan, Placement, CTS and routing – ECO flow – Signal Integrity Issues.		
Module:5	**Physical Design Verification**	**7 hours**
Timing Sign-off, Physical Signoff - DRC and LVS, ERC, IR Drop Analysis, and Antenna Checks		
Module:6	**Contemporary Issues**	**2 hours**
Industry Expert Guest Lectures		
	Total Lecture Hours:	**45 hours**

Text Book(s)

Vaibbhav Taraate, " **ASIC Design and Synthesis**", Springer, 1st Edition, **2021**
Sneh Saurabh, "**Introduction to VLSI Design Flow**", Cambridge University Press, 1st Edition, **2023**

Reference Books

Khosrow Golshan, "**PHYSICAL DESIGN ESSENTIALS: An ASIC Design Implementation Perspective**", Springer, 1st Edition, **2010**
Andrew B. Kahng, "**VLSI Physical Design: From Graph Partitioning to Timing Closure**", Springer, 1st Edition, **2022**
J. Bhasker and Rakesh Chadha, "**Static Timing Analysis for Nanometer Designs**", Springer, 1st Edition, **2010**
Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, " **VLSI Test Principles and Architectures**", The Morgan Kaufmann, 1st Edition, **2013**

Indicative Experiments

1. Design of Digital Architecture for the given specification - Design of SPI / Design of a simple CPU	4 hours
2. Logical Synthesis of Digital Architecture	4 hours
3. DFT synthesis and ATPG	4 hours
4. Netlist Optimization, GLS and Formal Verification	4 hours
5. Physical Design of Digital Architecture	10 hours
6. Physical Verification of Digital Architecture – DRC and LVS	4 hours
Total Laboratory Hours:	**30 hours**

Mode of Evaluation : Continuous Assessment Test, Quiz, Final Assessment Test, Presentaion

Recommended by Board of Studies :	30-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD304	VLSI Technology	3	0	2	4
Pre-requisite	BAEVD101 Electronic Devices	Syllabus Version			
		1			

Course Objectives

1. Introduce the fundamentals of VLSI manufacturing processes and technology
2. Understand the various patterning techniques and their limitations.
3. Gain a stronger grasp of thin film deposition and etching methods and understand the fundamental principles of metals used in gate and packaging applications

Course Outcomes

1. Illustrate crystal structure, lithography techniques, wafer exposure system concepts, types of resists etc.
2. Interpret thermal oxidation, diffusion and ion implantation techniques.
3. Apply thin film deposition and etching techniques.
4. Apply back-end technology to define contacts, interconnect, gates, source and drain, and measurement techniques to ensure the quality of designs.
5. Interpret process variations on the material/device properties

Module:1	Introduction	9 hours

Introduction to Semiconductor Manufacturing and fabrication (Si, III-V devices), Clean Room types and standards, Crystal structure, Czochralski growth method, Wafer preparation, and defects, Photolithographic Process, Photomask Fabrication, Comparison between positive and negative Photoresists, Exposure Systems

Module:2	Lithography and oxidation	10 hours

Characteristics of Exposure Systems, Baking, and development, Mask making, E-beam Lithography, Nano imprint lithography. The Oxidation Process, Nitridation, Masking Properties of Silicon Dioxide, Technology of Oxidation, Characterization methods, Segregation, Interfacial dopant pileup, oxidation-enhanced diffusion, and dopant-defect interaction

Module:3	Diffusion and Ion Implantation	8 hours

Basic concepts, Diffusion process and models, High energy and ultralow energy implantation, shallow junction formation & modeling, Electronic stopping, Damage production and annealing, RTA Process and dopant activation, Ion Implantation.

Module:4	Thin film deposition techniques	10 hours

Thermal and e-beam evaporation, DC Sputtering, RF sputtering Atomic Layer Deposition (ALD), Chemical Vapour Deposition (CVD) and its types (thermal, plasma-enhanced, metal-organic), Electrodeposition, Wet etching, Plasma etching, RIE, Etching of materials used in VLSI.

Module:5	**Metallization and packaging**	**6 hours**
Contacts, Vias, Multi-level Interconnects, Silicide gates and S/D regions, Reflow & planarization, Multi-chip modules, packaging and its types.		
Module:6	**Contemporary Issues**	**2 hours**
Contemporary Issues		
	Total Lecture Hours:	**45 hours**

Text Book(s)

R.C. Jaeger, "**Introduction to microelectronic fabrication**", Pearson, 1st Edition, **2013**

J.D. Plummer, M. Deal, P.D. Griffin, "**Silicon VLSI Technology: Fundamentals, Practice, Modeling**", Prentice Hall, 2nd Edition, **2009**

Wang Yangyuan, Jesse Jen-Chung Lou, Min-Hwa Chi, Chun-Zhang Chen, "**Handbook of Integrated Circuit Industry**", Springer Nature Singapore, 1st Edition, **2023**

Reference Books

S.A. Campbell, "**Fabrication Engineering at the Micro- and Nanoscale**", Oxford University Press, 1st Edition, **2013**

S.K. Ghandhi, "**VLSI fabrication principles**", John Wiley, 2nd Edition, **2009**

S.M. Sze, "**VLSI Technology**", Tata McGraw Hill, 2nd Edition, **2017**

Shubham Kumar, Ankaj Gupta, "**Integrated Circuit Fabrication**", CRC Press, 1st Edition, **2021**

Indicative Experiments

1. Silicon wafer dicing, pre-cleaning	2 hours
2. Oxidation of silicon wafer	4 hours
3. Evaporation of metal onto a substrate	4 hours
4. DC sputtering of metal onto a substrate	2 hours
5. Optical microscopy characterization of the deposited materials	2 hours
6. C-V characteristics of fabricated MOSFET/MOS Capacitor	2 hours
7. Introduction to oxidation modeling	2 hours
8. Modeling for SiO2 growth of various processes.	2 hours
9. Simulation study on diode/ BJT device structure	3 hours
10. Simulating the device characteristics of MOSFET	3 hours
11. Modeling the material structures and predicting their properties	4 hours
Total Laboratory Hours:	**30 hours**

Mode of Evaluation : Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Final Assessment, Presentaion	
Recommended by Board of Studies :	23-05-2025
Approved by Academic Council : No. 78	12-06-2025

Course Code	Course Title	L	T	P	C
BAEVD305	CAD for IC Design	3	1	0	4
Pre-requisite	NIL	**Syllabus Version**			
		1			

Course Objectives

Introduce the fundamentals of graph theory, graph algorithms, and computational complexity relevant to VLSI design automation.
Provide a comprehensive understanding of algorithms used in circuit partitioning, floorplanning, placement, routing, and clock tree synthesis.
Familiarize learners with the application of machine learning techniques in VLSI CAD.

Course Outcomes

Apply graph-theoretic and computational principles to model and solve problems in design automation.
Analyze partitioning strategies to evaluate design trade-offs and optimize system performance.
Analyze planning and placement methodologies by examining design constraints, cost functions, and optimization criteria.
Examine routing and timing strategies to assess interconnect efficiency and performance in system design.
Illustrate machine learning techniques to improve and optimize VLSI computer aided design automation.

Module:1	**Introduction**	**8 hours**

VLSI CAD Abstraction Levels, Algorithms and Complexity, Graph Theory Terminology, Graph Traversal/Search- Breadth First Search, Depth First Search, Topological Ordering, Minimum Spanning Tree- Kruskal's Algorithm, Prim's Algorithm, Shortest Paths in Graphs- Dijkstra's Algorithm.

Module:2	**Circuit Partitioning**	**6 hours**

Problem Formulation, Approaches to Partitioning Problem- Kernighan-Lin Algorithm (Weighted), Fiduccia Mattheyses Heuristic, Simulated Annealing.

Module:3	**Chip Planning and Placement**	**12 hours**

Problem Formulation for Chip Planning, Approaches to Floor Planning Problem- Wong-Liu algorithm, Stockmeyer, Sequence Pair . Problem Definition for Placement, Cost Functions and Constraints, Approaches to Placement- Min- cut Heuristic, Analytic Placement.		
Module:4	**Signal and Clock Routing**	**12 hours**
Problem Definition for Routing, Cost Functions and Constraints, Maze Routing Algorithms- Lee Algorithm, Power and Ground Routing, Global Routing- Routing Regions, Sequential Global Routing, Channel Routing- Problem Definition, Left-Edge Algorithm, Dogleg Algorithm, Switchbox Routing. Introduction to Area Routing, Net Ordering in Area Routing, Basic Concepts in Clock Networks, Modern Clock Tree Synthesis.		
Module:5	**Machine Learning for VLSI CAD**	**2 hours**
Preliminary Taxonomy for Machine Learning in VLSI CAD, Machine Learning for Datapath Placement, Machine Learning for Routability-Driven Placement, Machine Learning for Clock Optimization, Contemporary Issues.		
Module:6	**Contemporary issues**	**2 hours**
Guest lectures from Industries and R&D Organizations		
	Total Lecture Hours:	**42 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
Andrew B. Kahng, "**VLSI Physical Design: From Graph Partitioning to Timing Closure**", Springer, 2nd Edition, **2022** Ibrahim M. Elfadel, Duane S. Boning, and Xin Li, "**Machine learning in VLSI Computer-Aided Design**", Springer, 1st Edition, **2019**		
Reference Books		
Sadiq M. Sait and Habib Youssef, "**VLSI Physical Design Automation: Theory and Practice**", World Scientific Publishers, 1st Edition, **1999** Sung Kyu Lim, "**Practical Problems in VLSI Physical Design Automation**", Springer, 2nd Edition, **2011** Naveed A. Sherwani, "**Algorithms for VLSI Physical Design Automation**", Springer, 2nd Edition, **2012**		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Course Project, Case Study		

Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD306	Testing of VLSI Circuits	3	0	2	4
Pre-requisite	BEVD102 Digital System Design/ BAECE102 Digital logic Design/ BACSE103 Computation Structures/ BAITE101 Digital Logic Design and Computer Organization / BAEEE201 Digital Electronics	**Syllabus Version**			
		1			

Course Objectives

Establish a comprehensive understanding of the critical role testing plays in the VLSI lifecycle and the application of various fault models across design abstraction levels.
Equip students with the technical expertise required to integrate Structured Design for Testability (DFT) strategies into digital circuits, ensuring high-quality and robust hardware designs.
Foster advanced skills in developing test generation algorithms and fault simulation techniques for both logic and memory systems.

Course Outcomes

Illustrate various fault models and testing strategies that apply to different abstraction levels within the VLSI design flow.
Apply fault simulation and test generation algorithms to evaluate and test combinational circuits.
Apply DFT techniques to improve the testability of digital circuits, interconnects, and I/Os.
Utilize memory test algorithms and MBIST (Memory Built-In Self-Test) to test memory modules.
Apply Test compression techniques and test response compaction methods to reduce memory and test time.

Module:1	**Testing and Fault Modelling**	**9 hours**

Importance of testing - Testing during the VLSI lifecycle - Fault models: Stuck-at faults, Transistor faults, open and short faults, Delay faults and crosstalk, Pattern sensitivity and coupling faults, Analog fault models - Fault equivalence and fault collapsing - Levels of Abstraction in VLSI testing - Review of VLSI Test.

Module:2	**Fault Simulation and Test Generation**	**8 hours**

Fault Simulation: Serial, Parallel, Concurrent, and Deductive Fault Simulations. Test Generation: Combinational ATPG: D-Algorithm, FAN and PODEM.		
Module:3	**Design for Testability**	**13 hours**
Design for Testability: Ad-hoc approach, Structured approach - Scan cell designs, Scan architectures, Scan Design Rules, Scan Design Flow, Logic BIST: BIST Design Rules - Test Pattern Generation: LFSR - Output Response analysis: Signature Analysis. Board-level Testing: Digital boundary scan (IEEE Std.1149.1).		
Module:4	**Memory Testing**	**6 hours**
RAM Functional Fault Models and Test Algorithms - RAM Fault Simulation and Test Generation - Memory Built-In Self-Test.		
Module:5	**Test Data Compression and Response Compaction**	**9 hours**
Test Compression: Linear decompression-based schemes, Broadcast scan-based schemes - Test response compaction: Space compaction, Time compaction, Mixed time and space compaction. Introduction to post-silicon validation, Contemporary Issues.		
	Total Lecture Hours:	**45 hours**
Text Book(s)		
Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, "**"VLSI Test Principles and Architectures**", The Morgan Kaufmann, 1st Edition, **2015** M. Bushnell, Vishwani Agrawal, "**Essentials of Electronic Testing for Digital, Memory,and Mixed-Signal VLSI Circuits**", Springer, 2nd Edition, **2015**		
Reference Books		
Sebastian Huhn, Rolf Drechsler, "**Design for Testability, Debug and Reliability Next Generation Measures Using Formal Techniques**", Springer, 1st Edition, **2021** Laung-Terng Wang, Charles E. Stroud, Nur A. Touba, "**System-on-chip Test Architectures: Nanometer Design for Testability**", Morgan Kaufmann Publishers, 1st Edition, **2015**		
Indicative Experiments		
1. Model a given combinational circuit and perform fault collapsing to identify the equivalent stuck-at faults (SSFs) using a scripting language or EDA tool.		6 hours

2. Stuck-at-fault and IDDQ Testing by Simulation.	6 hours
3. DFT Synthesis of complex Sequential circuits: fixing DFT rule violation, Scan insertion.	4 hours
4. ATPG, Fault simulation and Analysis (Stuck-at-faults, Transition faults, at-speed test with OCC- LoC and LoS)	6 hours
5. Design a BIST controller using an LFSR (Linear Feedback Shift Register) for pattern generation and a MISR (Multiple Input Signature Register) for output response analysis.	4 hours
6. Design and simulate a Boundary Scan architecture for a simple IC, demonstrating the use of TAP Controller instructions for board-level interconnect testing.	4 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment, Course Project, Case Study	
Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD307	Low Power VLSI Design	3	1	0	4
Pre-requisite	BEVD102 Digital System Design/ BAECE102 Digital logic Design/ BACSE103 Computation Structures/ BAITE101 Digital Logic Design and Computer Organization / BAEEE201 Digital Electronics	**Syllabus Version**			
		1			

Course Objectives

Introducing the necessity of low power design in VLSI circuits.
Provide a broad insight into the methods used to confront the low power issue from lower level (circuit level) to higher levels (system level) of abstraction.
Design various low power VLSI circuits.

Course Outcomes

Interpret the probabilistic approaches for power estimation.
Apply architectural and algorithmic transformations to optimize power consumption at the system level.
Implement gate-level and circuit-level techniques for power reduction.
Analyze the usage of sleep transistors and power gating technique for minimizing leakage power.
Develop power-aware designs using Unified Power Form

Module:1	**Fundamentals of Power Dissipation and Power Estimation**	**12 hours**

Motivation, Sources of Power dissipation in Deep Submicron CMOS and FINFET Circuits - Static, Dynamic and Short circuit components, Low power design flow, Overview of power optimization at various levels. Theoretical background of power estimation, Calculation of Steady state probability- Algorithm for signal probability propagation- Shannon's decomposition- BDD, Transition probability, Conditional probability, Transition probability of correlated inputs, Transition density, Estimation of Switching activity.

Module:2	**System Level and Algorithm Level Power Optimization Techniques**	**10 hours**

Pipelining, Parallel Processing and retiming approaches for power minimization, Multiple supply voltage design - Challenges - Level shifters, Low power SRAM Design, Clock gating, Data gating, Bus Encoding techniques, Precomputation, Operator reduction and Operator substitution for low power.		
Module:3	**Gate Level and Circuit Level Power Optimization Strategies**	**6 hours**
Transistor variable re-ordering for power reduction, Gate resizing, Low power library cell design (GDI), Approximate computing for reducing power consumption in adders and multipliers, Synthesis of FSM for low power.		
Module:4	**Leakage Power Reduction and Power Gating Techniques**	**8 hours**
Leakage power reduction techniques for CMOS and FINFET based circuits, Sleep Transistors, Power gating - coarse grain and fine grain, Switch fabric, Isolation, Retention, Power down and wake up methods.		
Module:5	**UPF Based IC Design**	**7 hours**
Unified power format (UPF)- Necessity, basic syntax of UPF, Power intent for MSV and PSO, UPF for multi supply voltage design examples, Contemporary Issues.		
Module:6	**Contemporary**	**2 hours**
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
Kaushik Roy, Sharat Prasad, "**Low Power CMOS VLSI Circuit Design**", John Wiley and Sons Inc, 2nd Edition, **2010** Ajit Pal, "**Low Power VLSI circuits and Systems**", Springer, 1st Edition, **2015**		
Reference Books		
Gary K. Yeap, "**Practical Low Power Digital VLSI Design**", Springer, 1st Edition, **2010** Jan M. Rabaey, Massoud Pedram, "**Low power Design Methodologies**", Springer, 1st Edition, **2014** Dimitrios Soudris, Christrian Pignet, Costas Goutis, "**Designing CMOS Circuits for low Power**", Springer, 1st Edition, **2011** Keshab K.Parhi, "**VLSI Digital Signal Processing Systems: Design and Implementation**", Wiley Inter Science, 1st Edition, **1999**		

Michael Keating, David Flynn, Robert Aitken, Alan Gibbons, Kaijian Shi, "**Low power methodology manual: for system-on-chip design**", Springer Science and Business Media, 2nd Edition, **2008**	
Mode of Evaluation: Continuous Assessment Test, Quiz, Final Assessment Test, Course Based Design Project, Course Project	
Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD401	FPGA based System Design and Prototyping	3	0	2	4
Pre-requisite	BEVD102 Digital System Design/ BAECE102 Digital logic Design/ BACSE103 Computation Structures/ BAITE101 Digital Logic Design and Computer Organization / BAEEE201 Digital Electronics	**Syllabus Version**			
		1			

Course Objectives

Introducing the various FPGA architecture and prototyping guidelines
Provide insight to the hardcore and softcore processor architecture
Design the system using hardcore and softcore processor

Course Outcomes

Demonstrate the various FPGA Architecture and prototyping methods
Illustrate the architecture of hardcore and softcore processor
Apply the system design flow to design applications using softcore Processor
Apply the system design flow to design applications using softcore Processor
Experiment the system design using FPGA

Module:1	**FPGA Architecture and Prototyping**	**8 hours**

Generic Structure of FPGA - Configurable Logic and Adaptive Logic Module Architecture - Routing Architecture - I/O Architecture and Standard - Intel and Xilinx FPGA Architecture - Design for Prototyping - Design Guidelines - IP and prototyping

Module:2	**Hardcore and Softcore Processor Architectures in FPGA**	**7 hours**

Introduction to Soft-core and Hard-core Processors - Need for Embedded Processors in FPGA - Softcore Processor Architecture - Instruction Set and Features - Hardcore Processor Architecture - Processor Features - Instruction Set Architecture - Comparison of Soft-core and Hard-core Processors.

Module:3	**Configurable SoC Design and Hardware Software Codesign**	**8 hours**

Hardware/Software Co-design Flow - Functional Modeling and HW/SW Partitioning- System Design using Soft-core Processor -System Design using Hard-core Processor-

Configurable SoC Architectures - Case Study: EDA Design Flow for FPGA-based SoC Systems.		
Module:4	**System Design using softcore Processor**	**12 hours**
Softcore Processor System Design -Hardware-Software Co-design Methodology - On-chip Interconnects (Avalon /AXI) - Interrupts and Peripheral Integration - Real-Time Implementation of Algorithms-FIR Filter, Matrix Multiplication, Image Processing Algorithms: Image Thresholding, Edge Detection using Standard Operators, Pixel-level Arithmetic Operations.		
Module:5	**System Design using Hardcore Processor**	**8 hours**
Memory and Cache Considerations-Processing system (PS)- Processing Logic (PL) integration, Hardware acceleration using Programmable Logic-System Performance Considerations - Processing Algorithms: RGB Enhancement - Contrast / color enhancement		
Module:6	**Contemporary Issues**	**2 hours**
	Total Lecture Hours:	**45 hours**
Text Book(s)		
Wayne Wolf, "**FPGA-Based System Design**", Prentice Hall, 1st Edition, **2004** Zainalabedin Navabi, "**Embedded Core Design with FPGAs**", TATA McGraw Hill, 2nd Edition, **2011**		
Reference Books		
Doug Amos, Austion Lesea and Rene Ritcher, "**FPGA Prototyping Methodology Manual**", Synopsys, 1st Edition, **2011** Joseph Yu, "**System-on-Chip Design with Arm Cortex-M Processors**", ARM Education, 1st Edition, **2019**		
Indicative Experiments		
1. Hello World Application Using Softcore Processor		2 hours
2. LED and Switch Interfacing Using Softcore Processor		2 hours
3. Display Peripheral Interfacing (Seven Segment /LCD) and Real-Time Clock Display Using Softcore Processor		4 hours
4. Hello world application using hardcore Processor		2 hours

5. Processing System (PS)-Programmable Logic (PL) Interaction Using hardcore Processor	4 hours
6. Simple Hardware accelerator Using Programmable Logic (PL) with hardcore Processor	4 hours
7. FIR Filter Implementation using Hardware-Software Co-Design	4 hours
8. Matrix Multiplication and Performance Analysis	4 hours
9. Image Thresholding Using Hardware Acceleration	2 hours
10. Edge Detection Using Programmable Logic	2 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation: Continuous Assessment Test, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment, Course Based Design Project, Course Project, Case Study	
Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD402	Mixed Signal VLSI Design	3	1	0	4
Pre-requisite	BAEVD302 CMOS ANALOG IC DESIGN	**Syllabus Version**			
		1			

Course Objectives

Introduce the principles of sampling theory and the operation of switched-capacitor circuits used in mixed-signal systems.
Present the fundamentals, architectures, and performance metrics of analog-to-digital (ADC)and digital-to-analog (DAC) converters.
Develop an understanding of oversampling data converters, including noise-shaping concepts and system-level benefits.

Course Outcomes

Understand the principles of sampling circuits and switched-capacitor circuits.
Analyze the operation of static and dynamic comparators and compare their performance characteristics.
Understand the fundamentals of ADC operation and various architectures based on resolution, sampling rate.
Apply the fundamentals of DAC operation to various DAC architectures to determine output performance parameters such as INL and DNL.
Understand the concepts of oversampling converters, including noise shaping and related signal-processing techniques.

Module:1	**Sampling and Switched Capacitor Circuits**	**9 hours**

Basic Sampling Concepts and Circuits - Sampling Switches - Charge Injection, Clock Feedthrough - kT/C Noise - Bootstrapped Switch - Bottom Plate Sampling - Differential Sampling - Speed and Precision Considerations - Switched Capacitor Amplifiers - Switched Capacitor Integrators

Module:2	**Comparators**	**7 hours**

Basic Concepts - Amplification by Positive Feedback - Comparator Design Parameters - The StrongArm Comparator - Metastability - Noise - Offset Cancellation.

Module:3	**ADC Fundamentals and Architectures**	**10 hours**

Formulation of Quantization Error - ADC Performance Parameters - Offset, Gain Error, Differential and Integral Nonlinearity, Signal to Noise Distortion Ratio, Spurious Free Dynamic Range. ADC Architectures - Flash, Two Step Flash, Successive Approximation Register, Pipeline ADCs - Nonidealities.		
Module:4	**DAC Fundamentals and Architectures**	**10 hours**
DAC Performance Parameters - Static and Dynamic, Digital Codes in DACs, Clocking in DACs. DAC Architectures - Resistor Ladder, Current Steering, Pipeline, Capacitor DACs - Nonidealities.		
Module:5	**Oversampling ADCs**	**9 hours**
Basic Concepts - Discrete-Time Sigma Delta Modulator - Continuous-Time Sigma Delta Modulator -Design of Sigma Delta Modulators - SNR Calculation - Nonidealities, Contemporary Issues.		
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
Behzad Razavi, "**Analysis and Design of Data Converters**", Cambridge University Press, 1st Edition, **2025** R Jacob Baker, "**CMOS Circuit Design Layout and Simulation**", Wiley and IEEE Press, 3rd Edition, **2010**		
Reference Books		
R Jacob Baker, "**CMOS Mixed-Signal Circuit Design**", Wiley and IEEE Press, 2nd Edition, **2015** David Johns and Ken Martin, "**Analog Integrated Circuit Design**", John Wiley and Sons Inc, 2nd Edition, **2015**		
Mode of Evaluation: Continuous Assessment Test, Quiz, Final Assessment Test, Case Study		
Recommended by Board of Studies :		02-03-2026
Approved by Academic Council : No. 81		12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD308	Memory Devices and circuits	3	1	0	4
Pre-requisite	BAEVD101 - Electronic Devices	**Syllabus Version**			
		1			

Course Objectives

Learn the basics and detailed architecture of SRAMs, DRAMs, ROMs, and Flash Memories.
Model the memory faults and introduce the basic and advanced memory testing patterns.
Elaborate on the reliability and radiation effect issues of semiconductor memories.

Course Outcomes

Design SRAMs and DRAMs.
Design NVRAMs and Flash Memories.
Model and test memory faults, while incorporating DFT and BIST techniques for semiconductor memory testing.
Estimate the reliability of semiconductor memories, simulate and model radiation effects, and perform radiation hardening.
Contribute to the development of high-performance memory subsystems and use emerging memory technologies.

Module:1	**Volatile memories**	**7 hours**

Static Random Access Memory (SRAM) -SRAM cell structures, MOS SRAM architecture, MOS SRAM cell and peripheral circuit operation, SOI technology, Advanced SRAM architectures and technologies, soft error failure in SRAM, CAM, DRAM - DRAM technology development, CMOS DRAM, DRAM cell theory and advanced cell structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture.

Module:2	**Non-volatile memories**	**8 hours**

Masked ROMs, High density ROM, PROM, EPROM, Floating gate EPROM cell, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture, Ferroelectric Random Access Memories (FeRAMs), Phase Change Memory, Basic Magneto-resistive Random Access Memories (MRAMs) and STT-

MRAM-Memory Array Design-Peripheral circuits, Sense amplifier design, NVSim simulator.		
Module:3	**Memory Testing, Design for Test and BIST**	**10 hours**
General Fault Modelling - Read Disturb Fault Model - Precharge Faults - False Write Through, Data Retention Faults - Decoder Faults. Megabit DRAM Testing Nonvolatile Memory Modelling and Testing-IDDQ Fault Modelling and Testing Application Specific Memory Testing - Zero/one Pattern - Exhaustive Test Patterns-Walking, Matching and Galloping - Pseudo Random Pattern - CAM pattern. RAM Built-In Self - Test (BIST)-Weak Write Test mode - Bit Line Contact Resistance -PFET Test - Shadow Write and Shadow Read, BISR, BIRA.		
Module:4	**Reliability and Radiation Effects**	**8 hours**
General Reliability Issues- Hardening Process and Design Issues- Radiation Hardened Memory Characteristics. RAM Failure Modes and Mechanism-Nonvolatile Memory Reliability-Design for Reliability, Radiation Effects-Single Event Phenomenon (SEP)-Radiation Hardening Techniques.		
Module:5	**High-Performance Subsystem Memories, and Advanced Memory Technologies**	**12 hours**
Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories, High-Density Memory Packaging Technologies, Experimental Memory Devices, RRAM, Memory Hybrids and MCMs (2D)- Memory Stacks and MCMs (3D)-Memory MCM Testing and Reliability, Contemporary Issues.		
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
Shimeng Yu, "**Semiconductor Memory Devices and Circuits**", CRC Press, 1st Edition, **2022** R Dean Adams, "**High Performance Memory Testing: Design Principles, Fault Modelling and Self-Test**", Springer, 1st Edition, **2013**		
Reference Books		
Mode of Evaluation: Continuous Assessment Test, Quiz, Final Assessment Test, Seminar, Presentation, Course Based Design Project, Course Project		

Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD309	IC Packaging and Testing	3	1	0	4
Pre-requisite	BEVD305L VLSI Technology	**Syllabus Version**			
		1			

Course Objectives

Understanding of the multidisciplinary characteristic of IC packaging.
Analyze the relevance of a suitable package selection over the design features and feasibility
Interpret thermal management principles and reliability aspects in packaging.

Course Outcomes

Identify the kinds of packaging and their design flow.
Analyze the advanced packaging methods and various characteristics associated with the packaging.
Acquire fundamental knowledge on the interconnects, the materials associated with the packaging and substrates and modern industrial practices.
Understand the importance of thermal management in packaging and methods to manage them.
Analyze the topics associated with packaging reliability and failure analysis

Module:1	**Introduction to Semiconductor Packaging**	**9 hours**

Introduction to packaging, Categories of packaging- on-chip interconnect Vs first-level, second-level, system-level, 2D technology. Packaging design flow, Basic functions of a package, Traditional Packaging Technologies such as leaded and leadless packages, surface mount technology (SMT), ball grid array (BGA) and QFP. Use cases: for different packages - smartphone SoC, power modules, automotive ECU, server CPU, LED lighting, etc.

Module:2	**Advanced Packaging and Packaging Characteristics**	**9 hours**

Advanced packaging technologies -chip scale packaging, 3D high density packaging, PoP, System in package, package efficiency, Rent's Rule, Moore's law for packaging, 2.5D and 3D packaging technologies. Packaging Characteristics: Electrical characteristics, impedance and transmission line models -stripline, microstrip, and buried stripline, propagation delay models, Lattice diagrams for reflection analysis.

Thermal characteristics - thermal transport modes. (conduction, convection and radiation, newton's law of cooling).		
Module:3	**Packaging Interconnects materials and substrates**	**9 hours**
High-level wafer-to-package process flow: dicing, die attach, wire bond/flip-chip, molding/encapsulation, singulation, final test. Key assembly processes: wire bonding, die attach, encapsulation/sealing, cleaning, marking. Interconnect technologies used in advanced packaging, such as flip chip bumping, solder balls, and through-silicon vias (TSVs). Substrates and materials used in advanced packaging, such as organic substrates, build-up substrates, redistribution layers (RDLs), interposers, and fan-out substrates. Common package materials - Cu, Al, mold compounds, underfill, lead frame alloys.		
Module:4	**Thermal management**	**7 hours**
Importance of thermal management in advanced packaging, thermal management techniques, such as heat sinks, thermal interface materials (TIMs), and thermal vias. Design considerations for effective thermal management		
Module:5	**Testing and Reliability**	**11 hours**
Package-level testing, interconnect testing, and reliability testing, failure analysis techniques and strategies for ensuring package reliability, Thermomechanical and drop-shock reliability, Current stressing and electromigration driven failures. ESD sensitivity of bare die vs packaged parts and basic ESD handling. Moisture sensitivity levels (MSL), popcorn cracking, humidity and bias stress as standard qual stresses. Introduction to JEDEC-style Qual concepts (e.g., temp cycle, HAST/THB, HTOL). Overstress failures and wearout failures, electrical failures mechanisms, thermomechanical failure mechanisms, chemically induced failure mechanisms, multi-chip module yields, Contemporary Issues.		
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
Rao R. Tummala, "**Fundamentals of Device and Systems Packaging: Technologies and Applications**", McGraw Hill Education , 1st Edition, **2019** Greig W., "**Integrated circuit packaging, assembly and interconnections**", Springer Science and Business Media, 1st Edition, **2007**		
Reference Books		

Ephraim Suhir, Y.C. Lee, and C.P. Wong, "**Micro-and opto-electronic materials and structures: physics, mechanics, design, reliability, packaging.**", Springer , 1st Edition, **2007** Morris, J.E., "**Nanopackaging**", Springer, 1st Edition, **2018** Bath, J., "**Lead-free Soldering Process Development and Reliability**", John Wiley and Sons, 1st Edition, **2020** John H. Lau, "**Semiconductor Advanced Packaging**", Springer, 1st Edition, **2021**	
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Course Based Design Project, Course Project	
Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD310	Quantum Mechanics for Electronics Engineers	3	1	0	4
Pre-requisite	BAPHY108 -Semiconductor Physics	**Syllabus Version**			
		1			

Course Objectives

Educate the students on concepts of quantum theory and its importance.
Make the students understand the importance of quantum effects in devices.
Enable the students to apply quantum theory in the design of nanoscale devices.

Course Outcomes

Apply the concepts of quantum theory in semiconductor devices.
Understand the importance of Schrodinger wave equation & its applications.
Obtain the knowledge on quantum confinement effects.
Gain the knowledge in dispersion relations of electrons in solids.
Understand the perturbation theory and its applications.
Understand and apply the concept of quantum computation.

Module:1	**Elementary Principles and Problems in one dimension**	**12 hours**

Waves and particles: Light as particlesâ€"the photoelectric, Electrons as waves, Position and momentum, Expectation of the position, Momentum, Non-commuting operators. The Schrodinger equation - Waves and the differential equation, Density and current, The free particle, A potential step, The infinite potential well, The finite potential well, The triangular well, Coupled potential wells, The Ehrenfest theorem. Tunnelling Phenomena in Devices: The simple rectangular barrier, The tunnelling probability, A more complex barrier, The double barrier, Simple, equal barriers, The unequal-barrier case, Shape of the resonance, Approximation methodsâ€"the WKB method, Bound states of a general potential, Periodic potentials - Velocity, Superlattices Tunnelling, Tunnelling devices, A current formulation, The Landauer formula, The resonant tunnelling diode, Resonant interband tunneling. Single-electron tunneling, The double-barrier quantum dot.

Module:2	**The harmonic oscillator Basis functions operators and quantum dynamics**	**10 hours**

Periodic potential, Bloch oscillations, The wavefunction, Motion of the wave packet, A simpler approach with operators, Quantizing the LC Circuit, The vibrating lattice, Motion in a quantizing magnetic field, Connection with classical orbits, Adding lateral confinement. Position and momentum representation, operator properties: Time-varying expectations, Hermitian operators, On commutation relations. Linear vector spaces: matrix properties, The eigenvalue problem, Dirac notation. Fundamental quantum postulates: Translation operators, Discretization and superlattices, Time as a translation operator, Canonical quantization.		
Module:3	**Perturbation Theory**	**7 hours**
Stationary perturbation theory: The perturbation series, Some examples of perturbation theory - The Stark effect in a potential well, The shifted harmonic oscillator, Multiple quantum wells, Coulomb scattering. An alternative techniqueâ€"the variational method. Time-dependent perturbation theory: The perturbation series, Electron-phonon scattering, The interaction representation, Exponential decay and uncertainty.		
Module:4	**Motion in centrally symmetric potentials**	**7 hours**
The two-dimensional harmonic oscillator: Rectangular coordinates, Polar coordinates, Splitting the angular momentum states with a magnetic field, Spectroscopy of a harmonic oscillator. The hydrogen atom - The radial equation, Angular solutions, Angular momentum, Atomic energy levels, The Fermi-Thomas model, The Hartree self-consistent potential, Corrections to the centrally symmetric potential, The covalent bond in semiconductors.		
Module:5	**An Introduction to Quantum Computing**	**7 hours**
Qubits and Entanglement, Quantum Dots for Qubits, Josephson Junctions, Optical Qubits, Quantum gates, Quantum Communication and Cryptography.		
Module:6	**Contemporary issues**	**2 hours**
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
David K Ferry, "**Quantum Mechanics: An Introduction for Device Physicists and Electrical Engineers**", CRC Press, 3rd Edition, **2020** A. F. J. Levi, "**Applied Quantum Mechanics**", Cambridge University Press, 3rd Edition, **2023**		
Reference Books		

Jasprit Singh, "**Quantum Mechanics: Fundamentals and Applications to Technology**", Wiley VCH, 1st Edition, **2004**
Dennis M. Sullivan, "**Quantum Mechanics for Electrical Engineers**", Wiley and IEEE Press, 1st Edition, **2012**
David A. B. Miller, "**Quantum Mechanics for Scientists and Engineers**", Cambridge University Press, 1st Edition, **2008**
Richard L. Liboff, " **Introductory Quantum Mechanics**", Pearson Education Inc, 4th Edition, **2003**
Debdeep Jena, "**Quantum Physics of Semiconductor Materials and Devices** ", Oxford University Press, 1st Edition, **2022**

Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Course Project	
Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD403	Device Modeling and Characterization Techniques	3	0	2	4
Pre-requisite	BAEVD101 Electronic Devices	**Syllabus Version**			
		1			

Course Objectives

To provide strong foundational knowledge of semiconductor device physics and electrical characterization techniques for extracting material and device parameters.
To develop the ability to analyze and model PN junction diodes, Schottky diodes, and MOSFETs by correlating underlying physical mechanisms with experimentally measurable electrical characteristics.
To enable students to perform device simulation and compact modeling using TCAD tools and industry-standard SPICE models for nanoscale and multi-gate devices.

Course Outcomes

Apply electrical characterization techniques to extract key semiconductor material and device parameters.
Analyze and model PN and Schottky diodes using Iâ€“V and Câ€“V characteristics for parameter extraction and SPICE simulation.
Evaluate MOSFET characteristics and extract key parameters to assess short-channel and scaling effects.
Simulate semiconductor devices using TCAD and develop compact models for circuit-level applications.
Implement advanced compact models to analyze nanoscale and multi-gate device behavior.

Module:1	Semiconductor Characterization Techniques	10 hours

Electrical Characterization Techniques: Semiconductor resistivity measurements, Four-probe measurement technique, Hall effect measurement: carrier concentration and mobility extraction, Deep Level Transient Spectroscopy (DLTS), Carrier lifetime measurement techniques, I-V and C-V Measurement Techniques: DC I-V characterization of semiconductor devices, High-frequency and quasi-static C-V measurements, Extraction of: Threshold voltage (V_{th}), subthreshold slope, Drain Induced Barrier Lowering (DIBL), Carrier mobility, I_{ON}/I_{OFF} ratio. Interface and Reliability Characterization: Charge pumping method for interface trap density extraction, Low-frequency (1/f) noise measurements as indicator of oxide/interface quality.

Module:2	Diode Characterization and Modeling	8 hours
PN Junction Diode: Energy band diagram and carrier transport mechanisms, Ideal and non-ideal I-V characteristics, Extraction of diode parameters: saturation current, ideality factor, series resistance, C-V characteristics: depletion and diffusion capacitance, Built-in potential and doping profile extraction from C-V data, Schottky Barrier Diodes: Metal-semiconductor junction theory and barrier formation, Thermionic emission and barrier lowering, I-V characteristics and barrier height extraction, Comparison between PN and Schottky diodes (speed, leakage, switching applications), SPICE Modeling of Diodes: Large-signal and small-signal diode models, SPICE diode parameters and physical interpretation, Temperature dependence and breakdown modelling, High-level injection effects.		
Module:3	**MOSFET Characterization and Modeling**	**9 hours**
MOSFET Electrical Characteristics: Device structure and operating regions, C-V characteristics: accumulation, depletion, inversion, I-V characteristics: linear and saturation, Parameter extraction: V_{th}, mobility, transconductance, subthreshold slope, Effect of channel length and width, Series Resistance and Channel Effects, Source/drain series resistance modelling, Channel length modulation, Body effect and substrate bias influence, Analytical MOSFET Models: Gradual channel approximation, Pao-Sah model, Brews charge-sheet model, Short-Channel and Scaling Effects: Short-channel effects (SCE): DIBL, threshold roll-off, velocity saturation, Mobility degradation mechanisms, Narrow width effects, Scaling principles and challenges.		
Module:4	**TCAD and Compact Modeling**	**8 hours**
TCAD Fundamentals: Structure definition and meshing, Carrier transport models: Drift-Diffusion model, Energy Balance model, Hydrodynamic model, Mobility and recombination models, Compact Modeling Concepts: Need and motivation for compact modeling, Physics-based vs empirical compact models, MOSFET SPICE Level 1, Level 2, and Level 3 models, Extraction and interpretation of model parameters.		
Module:5	**Advanced SPICE Models for Modern Devices**	**10 hours**
Advanced MOSFET SPICE Models: BSIM3 model structure and parameters, BSIM4 model enhancements and parameter extraction, Multi-Gate and Nanoscale Devices: Multi-gate transistor fundamentals, FinFETs and Gate-All-Around (GAA) devices, Short-channel control in multi-gate architectures, Industry Standard Compact Models: BSIM-CMG for FinFETs and GAA devices, BSIM-IMG for independent multi-gate devices, Contemporary Issues.		
	Total Lecture Hours:	**45 hours**

Text Book(s)	
Yannis P. Tsividis, "**Operation and Modeling of the MOS Transistor**", McGraw Hill, 1st Edition, **1987** Nandita Das Gupta, and Amitava Das Gupta, "**Semiconductor Devices: Modelling and Technology**", PHI, 1st Edition, **2024**	
Reference Books	
Trond Ytterdal, Yuhua Cheng, and Tor A. Fjeldly, "**Device Modeling for Analog and RF CMOS Circuit Design**", John Wiley and Sons, 1st Edition, **2003** Chandan Kumar Sarkar, "**Technology Computer Aided Design: Simulation for VLSI MOSFET**", CRC Press, 1st Edition, **2018** T. A. Fjeldly, T. Ytterdal, and M. Shur, "**Introduction to Device Modelling and Circuit Simulation**", John Wiley, 1st Edition, **2008** Dieter K. Schroder, , 3th Edition, , "**Semiconductor Material and Device characterization**", Wiley Interscience IEEE press, 3rd Edition, **2006** Narain Arora, "**MOSFET modelling for VLSI simulation**", World Scientific Publishing Company, 1st Edition, **2007** A. B. Bhattacharyya, "**Compact MOSFET Models for VLSI Design**", Wiley, 1st Edition, **2009** Samar K. Saha, "**Compact Models for Integrated Circuit Design: Conventional Transistors and Beyond**", CRC Press, 1st Edition, **2017** G. Massobrio and P. Antognetti, "**Semiconductor Device Modelling with SPICE**", Tata McGraw Hill, 2nd Edition, **2010**	
Indicative Experiments	
1. (i) Introduction to TCAD tools. (ii) Creating p-n junction diode structure and simulating I-V characteristics using TCAD tools.	4 hours
2. Creating NMOS structure and simulation of ID-VGS and ID-VDS characteristics using TCAD tools and extraction of the following parameters.(i) Threshold voltage extraction.(ii) Subthreshold slop extraction.(iii) DIBL extraction.(iv) Body coefficient extraction.(v) Substrate and gate current extraction.(vi) Breakdown voltage extraction.(vii) Short channel device current.	4 hours
3. FinFET structure creation and extraction of DC parameters and AC parameters.	4 hours
4. (i) Introduction to SPICE tools.(ii) Level-1 diode model extraction.	2 hours
5. MOSFET-SPICE Level-1, Level-2 and Level-3 model extraction.	4 hours

6. MOSFET- BSIM3 MOSFET model extraction.	4 hours
7. MOSFET-BSIM-CMG and BSIM-IMG model parameter extraction.	4 hours
8. BSIM4/BSIM-BULK MOSFET model extraction.	4 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation: Continuous Assessment Test, Quiz, Final Assessment Test, Lab Continuous Assessment, Lab Final Assessment, Course Project, Case Study	
Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD404	Electronic Materials and Emerging Devices	3	1	0	4
Pre-requisite	BAEVD101 - Electronic Devices	**Syllabus Version**			
		1			

Course Objectives

Enrich the students with relevant concepts, principles, and properties of electronic materials which are constituents of modern semiconductor devices.
Provide the students the overview of classical theory, quantum mechanics and the modern theory of materials and carrier transport in semiconductor devices.
Introduce the students with scaling limits of transistors, alternate technologoes an emerging devices.

Course Outcomes

Understand electronic materials, crystal structures, and defects and analyze their influence on material properties.
Apply classical and quantum theories to explain properties of solids.
Analyze ferroelectric, piezoelectric, and magnetic material properties.
Evaluate carrier transport mechanisms in semiconductor devices and their impact on device performance.
Examine alternate FET technologies and emerging nanodevices.

Module:1	**Crystal structures and defects**	**10 hours**

Atomic mass and mole, Concept of lattice, Unit cell, Bravais lattices, Atomic mass and mole, Crystal planes and Miller indices, Interplanar spacing, Concept of reciprocal lattice, X-ray diffraction and Bragg's law, Czochralski growth. Defects: point and line defects, Schottky and Frenkel, dislocations, burger's vector, low angle grain boundaries, crystal surfaces and surface properties, effect of defects on leakage, mobility and lifetime; role of surface defects in MOS capacitors and interface traps.

Module:2	**Classical theory of solids**	**7 hours**

Classical theory, Drude model, temperature dependence of resistivity, Matthiessen's and Nordheims's rule, Hall effect and Hall devices, thermal conductivity, thermal resistance, electrical conductivity of semiconductors, relaxation time, drift velocity, drawbacks of classical theory, insulators and dielectrics, polarization, dielectric constant and dielectric losses, ferroelectric, piezoelectric, and magnetic materials.

Module:3	**Quantum mechanics and theory of solids**	**8 hours**
Need for quantum mechanics, wave particle duality, time-independent schrodinger equation, electronic band structure, free electron band, particle in a one-dimensional potential well, electron confinement and effect of layer thickness, band theory of solids, Kronig Penny model, semiconductors, effective mass, carrier concentration, density of states, Fermi-Dirac statistics, tunneling and its role in gate leakage.		
Module:4	**Carrier transport in semiconductor devices**	**8 hours**
Intrinsic and extrinsic semiconductors, conductivity, drift and diffusion current conduction, continuity equation, MOSFETs: threshold voltage, gate and drain current characteristics, short channel effects: channel length modulation, punch-through, mobility degradation, velocity saturation, drain-induced barrier lowering.		
Module:5	**Emerging Devices**	**10 hours**
Beyond planar CMOS: silicon-on-insulator MOSFET, multigate FETs: double gate FETs and FinFETs, new channel & material devices: III-V compound semiconductor devices, high electron mobility transistors; new switching mechanisms: negative capacitance FETs, magnetic tunnel junction		
Module:6	**Contemporary issues**	**2 hours**
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**

Text Book(s)

S. O. Kasap, "**Principles of Electronic Materials and Devices**", McGraw Hill Education, 4th Edition, **2021**

Donald A. Neamen, "**Semiconductor Physics and Devices**", McGraw Hill Education, 4th Edition, **2021**

Reference Books

J. P. Srivastava, "**Elements of Solid State Physics**", Prentice Hall, 4th Edition, **2014**

Ben G Streetman and Sanjay Kumar Banerjee, "**Solid State Electronic Devices**", Pearson, 7th Edition, **2016**

Adel S. Sedra, Kenneth C. Smith & Arun N. Chandorkar, "**Microelectronic Circuits: Theory and Applications**", Oxford University Press New York, 7th Edition, **2014**

Mode of Evaluation: Continuous Assessment Test, Quiz, Final Assessment Test, Seminar, Course Based Design Project, Case Study

Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD311	VLSI Architectures for Signal Processing	3	1	0	4
Pre-requisite	BEVD102 Digital System Design/ BAECE102 Digital logic Design/ BACSE103 Computation Structures/ BAITE101 Digital Logic Design and Computer Organization / BAEEE201 Digital Electronics	**Syllabus Version**			
		1			

Course Objectives

Understanding the basic idea of the signal flow graph and the interpretation between the signal flow graph and its architecture
Applying the advanced hardware realisation techniques to complex DSP algorithms.
Designing and implementing DSP architectures with a trade-off between area and speed.

Course Outcomes

Understand and apply the pipelining and parallel processing in DSP algorithms using the iteration bound.
Apply the architectural transformation techniques such as retiming, folding, and unfolding for optimizing cost and performance.
Understand and apply the systolic array approach in fast convolution algorithms.
Understand and apply numerical strength reduction in arithmetic operations.
Explore and appreciate the design considerations in hardware architecture for machine learning implementations.

Module:1	**Introduction to DSP Systems and Algorithms**	**9 hours**

Representation of DSP algorithms: block diagram, signal flow graph, data flow graph, dependence graph. Loop bound, Iteration bound - longest path matrix and minimum cycle mean algorithms. Pipelining and parallel processing of FIR filters, pipelining, and parallel processing for low power systems.

Module:2	**Architectural Transformation Techniques**	**9 hours**

Retiming - definitions and properties, Applications of retiming. Unfolding, Properties of Unfolding, Critical Path, Unfolding, and Retiming, Applications of Unfolding; Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures.

Module:3	**Fast Convolution and Systolic Architecture Design**	**10 hours**
Introduction, systolic array design methodology, FIR systolic arrays, selection of scheduling vector, matrix-matrix multiplication and 2D systolic array design. Fast convolution - CookToom algorithm, modified Cook-Toom algorithm, pipelined and parallel recursive filters - look-ahead pipelining in first-order IIR filters.		
Module:4	**Bit-Level Arithmetic and Numerical Strength Reduction**	**10 hours**
Bit-level arithmetic architectures - parallel multipliers with sign extension, parallel-carry ripple and carry-save multipliers, design of Lyon's bit-serial multipliers using Horner's rule. numerical strength reduction - sub-expression elimination, multiple constant multiplication, iterative matching		
Module:5	**Hardware Architectures for Machine Learning**	**7 hours**
Architectural approaches for implementing DNN: reduced precision of operations and operands (floating point to fixed point, reducing the bit width, nonuniform quantization, and weight sharing), reduce number of operations and model size (compression, pruning, and compact network architectures), Contemporary Issues.		
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
Keshab. K.Parhi, "**VLSI Digital Signal Processing Systems: Design and Implementation**", Wiley, 1st Edition, **2014**		
Reference Books		
V. Sze, "**Designing Hardware for Machine Learning** ", IEEE, 1st Edition, **2017** V. Sze, Y. Chen, T. Yang and J. S. Emer, "**Efficient Processing of Deep Neural Networks: A Tutorial and Survey**", IEEE, 1st Edition, **2017**		
Mode of Evaluation: Continuous Assessment Test, Quiz, Final Assessment Test, Case Study		
Recommended by Board of Studies :		02-03-2026
Approved by Academic Council : No. 81		12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD312	Semiconductor Optoelectronic Devices	3	0	2	4
Pre-requisite	NIL	**Syllabus Version**			
		1			

Course Objectives

Provide a strong foundation in semiconductor physics and optical processes governing optoelectronic devices.
Develop understanding of the design, operation, and characteristics of LEDs, laser diodes, photodetectors, and solar cells.
Expose students to advanced optoelectronic devices and their applications in modern technologies such as communication, energy, and sensing.

Course Outcomes

Explain the fundamental semiconductor physics and optical processes governing optoelectronic devices.
Analyze the operation, structures, and efficiency parameters of light-emitting devices such as LEDs and OLEDs.
Evaluate the principles, threshold conditions, and performance characteristics of semiconductor lasers.
Apply knowledge of semiconductor physics to assess the design and performance of photodetectors and solar cells.
Demonstrate understanding of advanced and emerging optoelectronic devices (SOAs, modulators, quantum well/dot, perovskite) and their applications.
Model, simulate, analyze, and evaluate the electrical and optoelectronic characteristics of semiconductor photonic devices (pâ€“n, pâ€“iâ€“n, APD, LED, Injection Laser Diode, and Solar Cell) using TCAD tools, and interpret their energy band diagrams and Iâ€“V characteristics under dark and illuminated conditions.

Module:1	**Fundamentals of Semiconductors and Optoelectronics**	**8 hours**

Semiconductor Physics Review: Energy band theory: intrinsic and extrinsic semiconductors, Direct and indirect bandgap semiconductors, Effective mass of electrons and holes, Carrier statistics and carrier concentration, Fermi level position and temperature dependence, Carrier Transport Mechanisms: Drift and diffusion currents, Mobility and conductivity, Einstein relation, Carrier generation and recombination mechanisms, Bulk recombination processes, Surface recombination and

surface states, Optical Processes in Semiconductors: Electron-hole pair generation, Optical absorption mechanisms (band-to-band, excitonic absorption), Spontaneous and stimulated emission, Radiative recombination, Non-radiative recombination mechanisms: Auger recombination, Shockley-Read-Hall (SRH) recombination, Photoluminescence fundamentals, Optical Properties of Semiconductors: Refractive index and dispersion, Optical gain and population inversion, Optical losses in semiconductors		
Module:2	**Optical Souces-1: Light Emitting Diodes**	**8 hours**
Principles of radiative recombination and spontaneous emission, LED structures and materials. Efficiency factors: internal quantum efficiency, extraction efficiency, LED characteristics:spectral response, modulation speed, Advanced LEDs: high-brightness LEDs, OLEDs, and quantum well LEDs.		
Module:3	**Optical Sources-2: Semiconductor Lasers**	**9 hours**
Stimulated emission and population inversion, Threshold condition and laser rate equations, Laser diode structures: homojunction, heterojunction, quantum well, DFB, DBR, Characteristics: L-I-V curves, modulation, linewidth, Applications in communications, sensing, and industry.		
Module:4	**Photodetectors and Solar Cells**	**9 hours**
Principles of photon detection. Photodiodes: p-n, p-i-n, avalanche photodiodes, Phototransistors and photoconductors, Noise sources in photodetectors, Solar cells: principles, materials, efficiency limits, tandem solar cells.		
Module:5	**Advanced Optoelectronic Devices and Applications**	**11 hours**
Modulators: electro-absorption and electro-optic modulators, Semiconductor optical amplifiers (SOAs), Quantum well and quantum dot devices, Emerging devices: perovskite optoelectronics, nanophotonic-based devices, Applications in optical communication, displays, sensing, LiDAR, Contemporary Issues.		
	Total Lecture Hours:	**45 hours**
Text Book(s)		
Pallab Bhattacharya, "**Semiconductor Optoelectronic Devices**", PHI Learning Pvt Ltd, 2nd Edition, **2012** P. Chakrabarti, "**Optoelectronic Devices and Optical Fiber Communication**", CBS Publishers and Distributers, 1st Edition, **2024**		
Reference Books		

S. O. Kasap, "**Optoelectronics and Photonics: Principles and Practices**", Pearson, 2nd Edition, **2013** John M. Senior, "**Optical fiber communications:Principles and Practice**", Pearson, 3rd Edition, **2014** Jasprit Singh, "**Semiconductor Optoelectronics: Physics and Technology, (First Indian Edition)**", McGraw-Hill, 1st Edition, **2019**	
Indicative Experiments	
1. Simulation of p-n junction photo diode-I-V characteristics (Energy band diagram, Dark Current and Current under illumination of light)	4 hours
2. Simulation of p-i-n photo diode-I-V characteristics ((Energy band diagram, Dark Current and current under illumination of light)	6 hours
3. Simulation of APD photodetector	6 hours
4. Simulation of LED	4 hours
5. Simulation of Injection Laser Diode (ILD)	6 hours
Total Laboratory Hours:	**30 hours**
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Lab Final Assessment, Course Based Design Project, Case Study	
Recommended by Board of Studies :	02-03-2026
Approved by Academic Council : No. 81	12-03-2026

Course Code	Course Title	L	T	P	C
BAEVD313	Hardware Accelerators for ML Applications	3	1	0	4
Pre-requisite	BEVD102 Digital System Design/ BAECE102 Digital logic Design/ BACSE103 Computation Structures/ BAITE101 Digital Logic Design and Computer Organization / BAEEE201 Digital Electronics	**Syllabus Version**			
		1			

Course Objectives

Introduce computational characteristics of ML workloads and motivation for hardware acceleration.
Familiarize students with architectural principles behind GPUs and domain-specific ML accelerators.
Enable reasoning-based design of ML accelerators under performance, energy and memory constraints.

Course Outcomes

Interpret computation and memory behavior of common ML workloads.
Analyze dataflow, parallelism, and memory hierarchy in architectures.
Examine CPUs, GPUs, and ML accelerators using architectural metrics.
Design a basic hardware accelerator for an ML kernel at an architectural level.
Evaluate accelerator designs using throughput, energy, and bandwidth metrics.

Module:1	**Introduction to Computer Architecture and ML Workloads**	**8 hours**

Foundations of Computer Architecture- Performance Metrics, Amdahl's law, Cache, Main Memory, Bandwidth vs Latency, Data Locality, Instruction level vs Data level parallelism, Basic Parallel Execution Models.ML Workloads Overview- ML applications, training vs inference. Need for acceleration, Common ML kernels, Limitations of general-purpose processors for ML, Evolution of hardware platforms

Module:2	**Parallelism and Dataflow**	**9 hours**

Types of parallelism, data reuse and locality, dataflow styles- stationary, output-stationary, row-stationary, tiling and blocking

Module:3	**GPU architectures**	**8 hours**

GPU execution model, programming abstraction, SIMD and SIMT, Memory Hierarchy, Performance characteristic of GPUS, matrix multiplication - CPU VS GPU		
Module:4	**Domain Specific ML Accelerators**	**10 hours**
Motivation, Systolic array architectures, Tensor Processing Architectures (TPUs), Trade-offs between flexibility, performance, energy-efficiency , Accelerator Design Examples.		
Module:5	**Memory Systems and Precision Optimization**	**8 hours**
Memory bandwidth challenges, On-chip Accelerators, Reduced precision arithmetic (FP16, INT8, INT4), Quantization concepts -hardware based, Impact of precision on performance, power and accuracy		
Module:6	**Contemprory Topics**	**2 hours**
Contemprory topics		
	Total Lecture Hours:	**45 hours**
	Tutorial Hours:	**15 hours**
Text Book(s)		
John L. Hennessy and David A. Patterson, "**Computer Architecture: A Quantitative Approach**", Morgan Kaufman, 7th Edition, **2025** Vivienne Sze , Yu-Hsin Chen , Tien-Ju Yang , Joel S. Emer, "**Efficient Processing of Deep Neural Networks**", Springer, 1st Edition, **2020**		
Reference Books		
William J. Dally and Brian Towles, "**Principles and Practices of Interconnection Networks**", Morgan Kaufman, 1st Edition, **2004** Norman P. Jouppi et al., "**In-Datacenter Performance Analysis of a Tensor Processing Unit**", ISCA, 1st Edition, **2017**		
Mode of Evaluation: Continuous Assessment Test, Digital Assignment, Quiz, Final Assessment Test, Course Based Design Project		
Recommended by Board of Studies :		02-03-2026
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