

### About SENSE:

SENSE at VIT was established for imparting state-of-the-art knowledge in Electronics and Communication Engineering and allied areas. The school has set up laboratories with excellent infrastructure in the areas of Electronics, Communication, VLSI, Embedded, Sensors and Nanotechnology. Faculties are actively involved in R&D activities and are working on research projects funded by government organizations like DRDO, ISRO (RESPOND), and DST.

### About Workshop:

This interactive and comprehensive workshop is designed for UG/PG students, research scholars and faculty members pursuing careers in research and development in VLSI and Embedded Systems. Participants will gain extensive knowledge in software development for custom RISC-V SoCs, covering topics ranging from automated hardware generation to bare-metal programming. This training culminates in a capstone project on Real-Time Operating System (RTOS) porting, empowering participants with advanced expertise in software integration across configurable, open-source hardware platforms.

### Course Content:

- Introduction to RISC-V, ISA and Programming Concepts
- Execution of Simple Programs and Resource Estimation
- Implementation of Matrix Multiplication, Convolution and FFT
- Verilog Coding of RISC-V and Functional Verification of ISA
- RISC-V FPGA Implementation
- UART Interface with RISC-V on FPGA
- SPI Interface with RISC-V on FPGA

**Date: 22<sup>nd</sup> to 23<sup>rd</sup> August 2026**

**Venue: TT 238**

**Time: 9:00 AM to 5:30 PM**

### Registration Fee:

**UG/ PG/ Research Scholars/ Faculty:  
Rs. 550+GST**

A certificate of participation will be awarded to all registered participants. Limited seats are available. Participants are encouraged to register at the earliest.

Use the link below to complete the online payment process: <https://events.vit.ac.in/>

### Advisory Committee:

**Dr. Jasmine Pemeena Priyadarisini**

Professor and Dean,  
School of Electronics Engineering (SENSE),  
Vellore Institute of Technology, Vellore, India.

**Dr. Sriadibhatla Sridevi**

Professor & Head,  
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### Coordinators:

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### Contact:

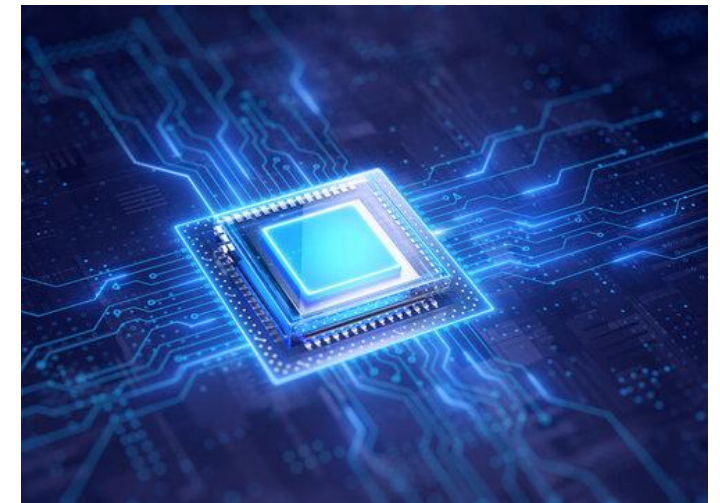
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## **2-day National Workshop “RISC-V on FPGA: Application Development & Porting” (hands-on) (22<sup>nd</sup>-23<sup>rd</sup> August 2026)**



**Organized By**

**Department of Micro & Nanoelectronics  
School of Electronics Engineering,  
VIT Vellore**