VALUE ADDED COURSE

Implementation of ML Algorithms with FPGA – VAC2515

About the Course

The value-added course, "Implementation of Machine Learning Algorithms with FPGA," aims to familiarize students with ML models for edge computing, the need for hardware acceleration, and the practical implementation of ML, NN, and DNN algorithms on FPGA platforms. The course includes hands-on sessions with FPGA design tools, HLS-based acceleration, optimization techniques such as quantization and pruning, and deployment workflows for real-time ML applications.

Highlights

- 30 Hours Training
- ML, NN, DNN, CNN Overview
- FPGA Design Basics & HLS Tools
- ML on FPGA: Regression, SVM, DT, RF
- Neural Networks & CNN Acceleration
- Optimization: Quantization, Pruning
- Case Study: CNN + OpenCV Use Cases
- Hands-on training using Artix 7, PYNQ-Z2, Xilinx Vivado, Google Colab, Jupyter notebook
- E-Certificate

(75% attendance + 60% marks)

Resource Person

- Dr S. Sivasankaran
- Dr. S. Sridevi
- Dr Antony Xavier Glittas
- Dr Prachi sharma
- Dr. Rajeev Pankaj Nelapati

Industry Expert

Dr. Muhammed Raees PC,
Edutecnicia, Kerala

Faculty Coordinators

Dr. S. Sridevi —
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Dr. Prachi Sharma —
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Dr. Rajeev Pankaj Nelapati
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Schedule

05.08.26 | 11:30 AM – 1 PM
22.08.26 | 9 AM – 1 PM
29.08.26 | 9 AM – 1 PM
05.09.26 | 9 AM – 1 PM
06.09.26 | 9 AM – 1 PM
10.10.26| 9 AM – 1 PM
11.10.26 | 9 AM – 1 PM
17.10.26| 9 AM – 1 PM
21.10.26| 11:30 AM – 1 PM

Seats Limited to 60 Participants

Registration

Fee: ₹500 (GST Included)

Link: https://events.vit.ac.in/

Venue

TT-312
VIT Vellore

Contact

9315043596 – Dr. Prachi Sharma
9043266364 – Dr. Rajeev Pankaj Nelapati

Advisory Committee

Dr. Jasmine Pemeena Priyadarsini,
Dean, SENSE

Dr. R.Sakthivel
Associate Dean, SENSE