



# VIT<sup>®</sup>

Vellore Institute of Technology

(Deemed to be University under section 3 of UGC Act, 1956)



## Industry Academia Conclave 2026

Bridging Innovation,  
Research & Impact

ONE-DAY HANDS-ON WORKSHOP ON

# RTL TO GDSII USING OPENROAD

A Complete Open-Source Physical Design Flow



**8<sup>TH</sup> SEPTEMBER 2026 (TUESDAY)**

**9:30 AM – 5:30 PM**



## OpenROAD



### OFFLINE MODE



**VENUE**

TT727, VIT Vellore



### WHO CAN PARTICIPATE?

- Faculty Members
- Researchers
- Industry Professionals
- UG/PG Students
- Participants from VIT



### KEY TOPICS

- Introduction to RTL Design and Digital Design Flow
- Overview of OpenROAD Flow
  - Synthesis, Floorplanning, Placement, CTS, Routing
- Design Rule Check (DRC) and Verification
- Static Timing Analysis (STA)
- Power, IR Drop and Signal Integrity Analysis
- GDSII Generation and Sign-off
- Hands-on Sessions using OpenROAD
- Interactive Q&A Session



### REGISTRATION FEES (Excluding GST)

EXTERNAL PARTICIPANTS

**₹ 600**

PARTICIPANTS FROM VIT

**₹ 400**

**REGISTER NOW!**



<https://events.vit.ac.in/>

Limited Seats | Register Early!



### RESOURCE PERSON

**Dr. Dhayala kumar**

Indian Institute of Information Technology  
Design & Manufacturing  
Kancheepuram, Tamilnadu, India



### WORKSHOP OUTCOMES

Participants will learn to:

- Understand and implement the complete RTL to GDSII flow using OpenROAD.
- Perform synthesis to GDSII generation using open-source tools.
- Analyze timing, power, and physical verification results.
- Gain hands-on experience with real design examples.



### E-CERTIFICATES

will be provided to all  
registered participants.

ORGANIZED BY

**SENSE**

SCHOOL OF ELECTRONICS ENGINEERING (SENSE)

**VIT VELLORE**

COORDINATORS

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For queries, please contact the coordinators



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