Chief Patron

Dr. G. Viswanathan , Chancellor

Patrons

Dr. Sankar Viswanathan
Vice President

Dr Sekar Viswanathan
Vice President

Dr G.V. Selvam
Vice President

Advisors

Ms Kadhambari S
Viswanathan AVP,VIT

Dr.Kanchana Baskaran
Vice Chancellor

Dr.Partha S Mallick
Pro- Vice Chancellor

Conveners

Dr. M. Jasmin Pemeena
Priyadarsini, Dean, SENSE

Dr. Sriadibhatla Sridevi
HoD, MNE, SENSE

About VIT

It was established under Section 3 of the University Grants Commission (UGC) Act, 1956, and was founded in 1984 as a self-financing institution called the Vellore Engineering College. The Union Ministry of Human Resources Development conferred University status on Vellore Engineering College in 2001. The University is headed by its founder and Chancellor, Dr. G. Viswanathan, a former Parliamentarian and Minister in the Tamil Nadu Government. In recognition of his service to India in offering world class education, he was conferred an honorary doctorate by the West Virginia University, USA. The VIT Vellore is ranked 14th as university, 16th in engineering, and 14th in research in NIRF 2025 rankings. In QS World University Rankings by Subject 2026, VIT is ranked 119th in the world. The global standards set at VIT in the field of teaching and research spur us on in our relentless pursuit of excellence. In fact, it has become a way of life for us. The highly motivated youngsters on the campus are a constant source of pride. Our Memoranda of Understanding with various international universities are our major strength. We look forward to meeting you here at VIT.

School of Electronics Engineering

School of Electronics Engineering (SENSE) at Vellore Institute of Technology, Vellore was established for imparting state-of-the-art knowledge in Electronics and Communication Engineering and allied areas. The school offers B.Tech programs in Electronics and Communication Engineering, Electronics Engineering (VLSI Design and Technology, and Electronics and Computer Engineering. The B.Tech. Electronics and Communication Engineering is accredited by the Engineering Accreditation Commission of ABET, http://www.abet.org. The school also offers M.Tech programs in VLSI Design, Embedded Systems, and Automotive Electronics. Students who are eligible are placed on campus and many of them are placed in core companies every year. The laboratories of the school are equipped with all industry standard simulation tools in the fields of Electronics, Communication, VLSI, Embedded, Sensors, and Nanotechnology. The School has many industry sponsored advanced laboratories for research and development.

VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

Five Days Workshop On

Device to Silicon : TCAD & RTL to GDS II Hands On

30th Sep 2026 to 4th Oct 2026

Organized by

Department of Micro and Nanoelectronics
School of Electronics Engineering
Vellore Institute of Technology
Vellore

Venue: TT 727, VIT , Vellore - 632014

Time : 09:30 AM – 05:00 PM

30th Sep 2026 to 4th Oct 2026

Registration : events.vit.ac.in (by 25/09/2026)

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Device to Silicon : TCAD & RTL to GDS II Hands On

30th Sep 2026 to 4th Oct 2026

About the Program

As we are at the smaller technology nodes, the semiconductor industry is looking for novel devices to suppress the device level non-idealities. In this context, the TCAD modeling plays a vital role in the understanding and research of device physics. Beside this, EDA tools are significant to build the understanding and to develop the workforce in the field of VLSI Design. Unlike other simulators, industry standard TCAD and EDA tools needs a special training. This hands-on workshop offers such training on Sentaurus TCAD (from Synopsys) and Cadence EDA tool suite.

Target Audience

Faculty, research scholars, and students from various engineering colleges of India. The number of participants are limited to 50.

Topics to be addressed :

Using Sentaurus TCAD from Synopsys

⇒ Sentaurus TCAD workflow (SDE and SDEVICE)
⇒ Physics and TCAD modelling of advanced devices
⇒ Parameter extraction using SVISUAL
⇒ Simulation of Short-channel effects and non-idealities
⇒ Devices for high-speed switching circuits

Topics to be addressed :

Using Cadence

⇒ RTL Design and Simulation
⇒ Synthesis and low power synthesis Using Cadence genus Compiler
⇒ Physical aware synthesis and DFT
⇒ Block and Top Level P&R Using Cadence Innovus
⇒ STA Using Timing Engine

Internal Resource Persons

Dr. Sriadibhatla Sridevi
Dr. Sakthivel R
Dr. Sandeep Moparthi
Dr. Ravi S
Dr. Rajeev Pankaj Nelapati
Dr. Ragunath

External Resource Persons

Dr. Ramkumar, RamIC Technologies, Bangalore

Registration and Payment link: events.vit.ac.in

Last Date for Registration: 25/09/2026

*** Paid accommodation will be provided.**

Registration Fees :

Registration fee includes lunch and snacks.

Faculty / Industry persons: Rs. 2500 + GST

Research scholars /UG & PG Students: Rs. 2000 + GST

Note : UG students only from 3rd / 4th year are eligible.

Coordinators

Dr. Ravi.S
Dr. Sandeep Moparthi
Dr. Rajeev Pankaj Nelapati

e-mail: msravi@vit.ac.in Contact: 97 9015 5650
sandeep.moparthi@vit.ac.in Contact: 6303423759

Program schedule:

Date	Forenoon	Afternoon
30-09-2026	Familiarization of Sentaurus TCAD & Device structure using SDE	Device Physics and modelling with SDEVICE (non-idealities)
01-10-2026	Parameter extraction using SVISUAL	Hands-on with Sentaurus TCAD (Advanced devices)
02-10-2026	RTL Design & Simulation (Cadence NClaunch)	RTL Synthesis (Cadence genus)
03-10-2026	Gate level Simulation (Cadence NC+Genus)	Functional verification using Cadence LEC , STA using Cadence Tempus
04-10-2026	Physical Design using Cadence Innovus	Mini Project

Venue: TT 727, Time : 09:30 AM – 05:00 PM

30th Sep 2026 to 4th Oct 2026

Department of Micro and Nanoelectronics
School of Electronics Engineering