

# AI × VLSI CAD

*From Algorithms to Tool-Driven Chip Design | A Two-Day Workshop*

Presented by **V-SPACE & Gravitas**

V-SPACE: VIT – Semiconductor Prototyping, Assembly, Characterization & Engineering Centre

**"Learn VLSI CAD. Build with EDA tools. Add AI. Prove the result."**

## ABOUT THE WORKSHOP

Learn how modern AI systems can interact with VLSI CAD algorithms and EDA tools to solve real hardware-design problems — through a closed loop:

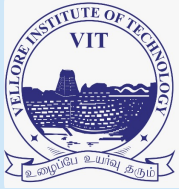
**Problem → Algorithm → Tool → Measurement → Feedback → Improvement**

**Day 1** builds the foundations across three sessions — VLSI CAD algorithms, real EDA workflows, and closing the AI–EDA feedback loop.

**Day 2** is an open-ended engineering challenge, where teams build their own intelligent EDA system across four tracks.

## WHAT YOU'LL WALK AWAY WITH

- A working understanding of VLSI CAD algorithms — graph methods, partitioning, floorplanning, placement, and routing
- Hands-on experience with real EDA tools (Verilator, Yosys, Icarus Verilog)
- A functioning AI-to-tool feedback loop, not just AI-generated code
- A completed AI + VLSI mini-project: source code, README, tool outputs, results, and a short demo



## DAY 1 — FOUNDATIONS: VLSI CAD + AI + EDA

### SESSION 1 — VLSI CAD ALGORITHMS

- Circuit representation as graphs; BFS/DFS, topological ordering, MST, Dijkstra
- Partitioning: Kernighan–Lin, Fiduccia–Mattheyses, simulated annealing
- Floorplanning, placement, routing, timing closure, cost functions
- **Hands-on:** model a netlist as a graph, implement algorithms, solve a partitioning problem

**Tools:** Python, NetworkX, NumPy, Matplotlib, Jupyter, Git

### SESSION 2 — REAL EDA WORKFLOW

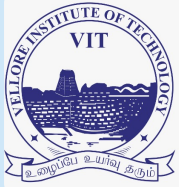
- RTL/netlist representation; verification vs. synthesis
- Reading EDA/compiler reports; identifying root causes
- Area, timing, congestion, wirelength as measurable outcomes
- **Hands-on:** debug intentionally flawed designs; validate fixes against real tools

**Tools:** Verilator, Icarus Verilog, Yosys, Git  
(optional: OpenROAD, KLayout, Magic, ngspice)

### SESSION 3 — AI + EDA CLOSED LOOP

- From "Prompt → Code" to "Prompt → Candidate → EDA Tool → Error/Metric → AI Feedback → Verified Result"
- Tool calling, automated repair, human-in-the-loop verification
- **Hands-on:** build a mini AI-assisted hardware workflow — spec → RTL → run → analyze → repair → re-run

**Tools:** Python + LLM API or local Qwen model + Verilator/Yosys



## DAY 2 — CHALLENGE: BUILD AN INTELLIGENT EDA SYSTEM

### CHALLENGE TRACKS

- **1. EDA Error Intelligence** — parse logs, classify errors, find root causes, suggest fixes, produce a structured report
- **2. VLSI CAD Optimization** — optimize wirelength, congestion, area, balance, and timing using graph/heuristic/ML methods
- **3. RTL / SVA / UVM Assistant** — generate RTL, assertions, and UVM components, validated by a real tool
- **4. AI EDA Agent** (most advanced) — an agent that selects tools, executes, diagnoses, repairs, and verifies

### TECHNICAL STACK

**Core:** Python, Git, Jupyter, NetworkX, NumPy, Matplotlib

**Digital EDA:** Verilator, Yosys, Icarus Verilog

**Physical design exposure:** OpenROAD, KLayout, Magic, Netgen

**AI:** local Qwen coder model or approved API model, structured tool calling

**Optional advanced** (institution-permitting): Cadence, Synopsys, ngspice

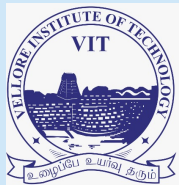
### EVENT DETAILS

Every team must deliver:

- A working implementation, reproducible on a fresh machine
- Tool evidence: compile/simulation results, logs, before/after metrics
- Structured, machine-readable output
- A clear distinction between AI suggestion and verified engineering result

*Outstanding solutions may be considered for continued participation in advanced VLSI-AI research and engineering projects, subject to institutional processes.*

| Day   | Focus                                                                                       |
|-------|---------------------------------------------------------------------------------------------|
| Day 1 | Foundations — VLSI CAD algorithms, real EDA workflow, and building the AI + EDA closed loop |
| Day 2 | Open challenge — teams design and build their own intelligent EDA system across four tracks |



**VIT**<sup>®</sup>  
**Vellore Institute of Technology**  
 (Deemed to be University under section 3 of UGC Act, 1956)



## REGISTRATION & EVENT DETAILS

### ELIGIBILITY & SCHEDULE

- ♦ **Open to:** All Undergraduate (UG) students
- ♦ **Event dates:** 12–13 September
- ♦ **Format:** Two-day, in-person workshop
- ♦ **Venue:** TT 727

### REGISTRATION FEE

**₹500**

per individual participant

- ♦ Registration is on an individual basis
- ♦ Seats are limited — register early to confirm your spot

| Detail           | Information                             |
|------------------|-----------------------------------------|
| Eligibility      | Open to all UG (undergraduate) students |
| Event Dates      | 12–13 September                         |
| Venue            | TT 727                                  |
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