



# WORKSHOP ON LOW POWER SEMICONDUCTOR DEVICE SIMULATIONS USING TCAD



**DATE**  
11/10/2026



**VENUE**  
TT-237A



**MODE OF CONDUCT**  
Hybrid

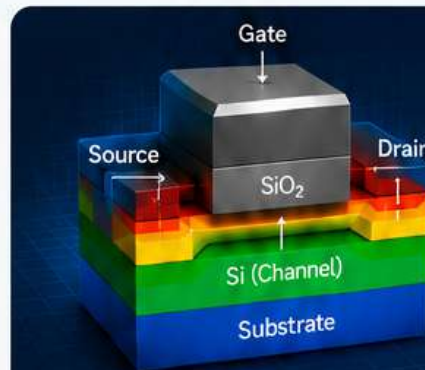


**TIME**  
10.00 AM – 5.00 PM



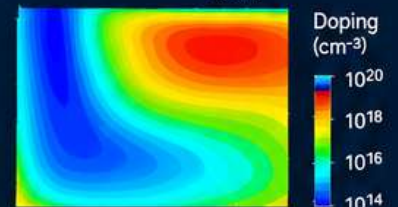
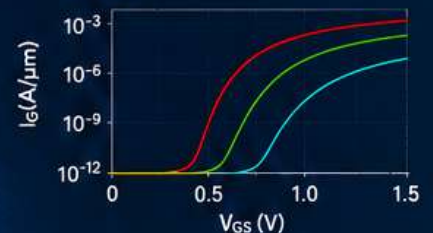
## OBJECTIVES

- 1 Familiarization of Device TCAD Simulations
- 2 Calibration and benchmarking of low power semiconductor devices using IRDS
- 3 Physics-based simulations and data extraction using hands-on sessions



- ✓ Physics-Based Modeling
- ✓ Low Power Device Analysis
- ✓ Data Extraction & Visualization
- ✓ Hands-on TCAD Sessions

## TCAD



## EXPERTS

### Dr. Rajesh Saha (Senior Member, IEEE)

is an Assistant Professor in the Department of Electronics and Communication Engineering, NIT Silchar. He has **150+ journal publications** in reputed IEEE, Elsevier, Springer, and other journals and has filed 3 patents. He has completed a **SERB-SRG sponsored project**, been recognized among the **World's Top 2% Scientists in Nanoscience & Nanotechnology (2023, 2024, 2025)** by Stanford University and Elsevier, and received the **IEI Young Engineers Award 2022-23** from The Institution of Engineers (India). His research interests include **Nanoelectronics Device Modeling and Simulation and Biosensors**.

### Dr. Rupam Goswami (Senior Member, IEEE)

is an Assistant Professor in the Department of Electronics and Communication Engineering, Tezpur University, India. He has research experience in **semiconductor device modeling and simulation**, with expertise in **TFETs, FinFETs, TFTs, advanced MOS devices, memristors, and charcoal electronics**. He is a recipient of the **Young Scientist Award 2021** by **DST, Government of Assam**, and the founder of **SemE-Hub**, a repository-cum-blog on computational programs for semiconductor devices and allied domains.

### Dr. Suman Kumar Mitra

is a SoC Physical Design Engineer at Altera, working on **3 nm FinFET FPGA** physical design and SoC power sign-off. Previously, he worked at Quest Global on **sub-7 nm technology nodes** of TSMC and Samsung and served as an Assistant Professor at HBTU Kanpur for 3.5 years. He holds a **Ph.D. in Microelectronics** from NIT Silchar, with research on **SOI TFETs**, and has published journal/conference papers and book chapters. He has also delivered **20+ invited lectures** at reputed institutions across India.



## ABOUT SENSE

SENSE at VIT was established for imparting state-of-the-art knowledge in Electronics and Communication Engineering and allied areas. The school has set up laboratories with excellent infrastructure in the areas of Electronics, Communication, VLSI, Embedded, Sensors and Nanotechnology. Faculties are actively involved in R&D activities and are working on research projects funded by government organizations like DRDO, ISRO (RESPOND), and DST.

### REGISTRATION FEE

UG/PG/Research Scholars/ Faculty:

**Rs. 200 + GST**

A certificate will be issued to all the registered participants. Use following link to make online payment.

<https://events.vit.ac.in/>



## ADVISORY COMMITTEE

### Dr. Jasmine Pemeena Priyadarisini

Professor and Dean,  
School of Electronics Engineering (SENSE),  
Vellore Institute of Technology,  
Vellore, India

### Dr. Kannadassan D

Professor & Head,  
Department of Communication Engineering,  
School of Electronics Engineering (SENSE),  
Vellore Institute of Technology,  
Vellore, India

### Dr. Sundar S

Professor & Head,  
Department of Embedded Technology,  
School of Electronics Engineering (SENSE),  
Vellore Institute of Technology,  
Vellore, India



## CO-ORDINATORS

### Dr. Shanidul Hoque

Associate Professor,  
School of Electronics Engineering (SENSE),  
Vellore Institute of Technology,  
Vellore, India – 632 014.

### Dr. Bijaylaxmi Das

Assistant Professor,  
School of Electronics Engineering (SENSE),  
Vellore Institute of Technology,  
Vellore, India – 632 014.



## CONTACT



+91-9401408475



shanidul.hoque@vit.ac.in



+91-8984764021



bijaylaxmi.das@vit.ac.in

