VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

School of Electronics Engineering
Innovate | Collaborate | Create Impact

SENSETRONICS

THE ECE MAGAZINE — 2024

Connecting Ideas to *Innovations*



- **DEAN'S MESSAGE** — Pioneering Innovation for a Smarter Tomorrow
- **RECOGNITIONS** — Accolades that Inspire
- **AWARDS & ACHIEVEMENTS** — Celebrating Excellence
- **HACKATHONS & STARTUPS** — From Ideas to Impact
- **CREATIVE CORNER** — A Space for Creativity and Expression

ELECTRONICS | COMMUNICATIONS | PHOTONICS | SIGNAL PROCESSING | EMERGING TECHNOLOGIES

CONTENTS

1 **Dean's Message** **3**

2 **ECE Anthem** **4**

3 **Collaborations & Outreach** **5**

Events at a Glance 2024 ..... **6**

a. AIIoT 2024 · 3rd IEEE International Conference on AI for IoT **7**

b. VDAT 2024 · 28th IEEE Symposium on VLSI Design and Test **10**

c. Industry Academia Conclave 2024 · Next Generation Communication **14**

MoU Reports · Nokia and Marvell 18

4 **Emergent Trends & Technology** **21**

a. Upcoming Technologies **22**

AI TRiSM and Quantum Security 22

Emerging Trends in VLSI 2024 24

Reconfigurable Intelligent Surfaces: Transforming Wireless Communication Towards 6G 26

Extended Reality: Technology, Construction and Applications 29

Autonomous Systems Beyond Roads: Unmanned Aerial and Underwater Vehicles 33

5 **Alumni Spotlight** **37**

6 **Creative Corner** **38**

a. Poems **39**

7 **Editorial Team** **44**

Dean's Message

Dear VITians,

I trust this message finds you in good health and high spirits. Today, I am delighted to bring you important updates and announcements concerning our esteemed institution's School of Electronics Engineering. In light of the ever-evolving landscape of electronics engineering, we have embarked on a thorough review of our curriculum. Our goal is to ensure that our programs remain at the forefront of technological advancements, equipping our students with the skills and knowledge essential for success in the industry. Anticipate exciting changes in our course offerings, upgraded laboratory facilities, and enriched project-based learning opportunities.

In our commitment to fostering innovation and facilitating groundbreaking research, we have actively pursued collaborations with industry partners and secured additional funding for research projects. These efforts will provide our faculty and students with expanded opportunities to delve into cutting-edge technologies, engage in multidisciplinary research endeavors, and contribute to addressing real-world challenges. To bridge the gap between academia and industry, we are proactively establishing partnerships and collaborations with leading technology companies. These collaborations will enable our students to gain practical insights through internships, industrial training programs, and guest lectures from industry experts.

We firmly believe that these interactions will enhance your professional growth and help you establish valuable industry connections. I am thrilled to present the 1st issue of magazine, "SENSETRONICS", by the School of Electronics Engineering (SENSE) for the year of 2024. This edition showcases the well-deserved honors and recognitions bestowed upon both faculty and students within the SENSE family for the period of January to December 2024. I extend my heartfelt gratitude to all members of the SENSE family for their unwavering support and contributions that have made this magazine possible. Your continued support is deeply appreciated, and we eagerly anticipate realizing the institute's mission and vision. Thank you, and we look forward to an exciting journey ahead.

With best wishes,



Dr Sivanantham S
Professor & Dean
School of Electronics Engineering (SENSE)
Vellore Institute of Technology, Vellore.

ECE ANTHEM

for Modern Semiconductor Materials

Innovating Today, Empowering Tomorrow!

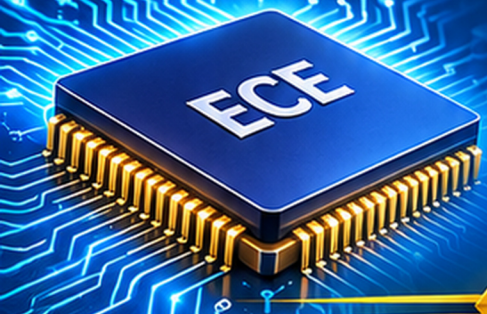




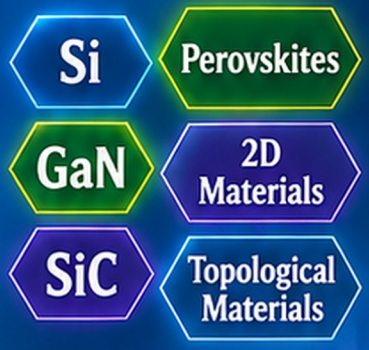
Verse 1 – The Spirit of Innovation

From silicon's dawn to quantum's promise,
We explore, design and innovate;
With modern **semiconductor materials**,
We build a smarter, brighter future.

Verse 2 – The Materials Revolution



Perovskites, 2D and wide-bandgap,
From nano to beyond, we strive;
In every layer, every junction,
We power **progress**, keep dreams alive.



Chorus – The ECE Pride

ECE, our pride, our passion,
Bridging technology and tomorrow;
With modern **semiconductor materials**,
We spark innovation forever!



Verse 3 – A Sustainable Tomorrow

Let's engineer a sustainable world,
With smart chips and **green solutions**;
Together, in ECE's united spirit,
We lead the next revolution!





ECE – Innovating Today, Empowering Tomorrow!

COLLABORATIONS & OUTREACH

- AIIOT 2024
- VDAT 2024
- INDUSTRY ACADEMIA CONCLAVE 2024

Events at a Glance 2024

Overview and summary of events hosted by the School of Electronics Engineering (SENSE), VIT Vellore

During 2024, SENSE brought industry experts, international researchers and academia together through three flagship events. Each report that follows gives the event details, the speakers and sessions, and photographs. The MoUs signed with Nokia and Marvell, which strengthen the school's industry collaboration, are reported with the Industry Academia Conclave.

#	Event	Date	Mode / Venue	Highlights
1	3rd IEEE International Conference on AI for Internet of Things (AIIoT 2024)	3–4 May 2024	Hybrid, VIT Vellore	Five technical tracks, a Women in Engineering track, special sessions by FICORE (Finland) and UTeM (Malaysia), and 12 keynote speakers from five countries
2	28th IEEE International Symposium on VLSI Design and Test (VDAT-2024)	1–3 September 2024	In person, VIT Vellore	Theme: Emerging Technologies for VLSI Design Ecosystem; supported by the VLSI Society of India; proceedings in IEEE Xplore
3	5th Industry Academia Conclave – Next Generation Communication'24	13 September 2024	In person, Ambedkar Auditorium, TT727 and TT312	320 participants, 12 industry speakers across four sessions; MoUs with Nokia and Marvell

Why these events matter

- Industry exposure: students and faculty interacted with practitioners from NXP, Marvell, Nokia, Samsung, Ericsson, Cisco, Synopsys, Cadence and many others.
- Global outlook: AIIoT 2024 brought keynote speakers from Finland, Malaysia, Serbia, Canada and the USA.
- Career pathways: talks, tutorials, design contests and internships linked to MoU partners give postgraduate students routes into industry.
- Alignment with SDG 4 (Quality Education) and SDG 9 (Industry, Innovation and Infrastructure).

AIIoT 2024: 3rd IEEE International Conference on AI for Internet of Things

Overview

AIIoT 2024, the 3rd IEEE International Conference on Artificial Intelligence for Internet of Things, ran on 3–4 May 2024 in hybrid mode. It was hosted by the School of Electronics Engineering (SENSE) at Vellore Institute of Technology (VIT), Vellore, Tamil Nadu, India.

Item	Detail
Event	3rd IEEE International Conference on AI for Internet of Things (AIIoT 2024)
Dates	3–4 May 2024
Mode	Hybrid (in person and online)
Host	School of Electronics Engineering, VIT, Vellore – 632014, Tamil Nadu
General Chair	Dr. Sivanantham S., Professor, SENSE, VIT
Conference Chair	Dr. Arun M., Professor, SENSE, VIT
Contact	chair.aiiot@vit.ac.in, +91 95978 12810, +91 88383 37267
Submissions	https://vit.ac.in/AIIoT2024/

Inauguration and souvenir release

The conference opened with a traditional lamp-lighting ceremony, followed by the release of the conference souvenir. Both were held in front of the AIIoT backdrop, which carries the VIT logo and the School of Electronics Engineering name.



- **Lamp lighting:** A senior guest lit the ceremonial brass lamp, decorated with jasmine garlands, while faculty, organizers and a foreign guest stood alongside. Several attendees wore conference lanyards.
- **Souvenir release:** Eight people stood behind the dais table and held up copies of the souvenir together. The table placards read Dean–SENSE, Vice President, Chief Guest, Chancellor, Guest of Honour and Pro-Vice Chancellor, showing the university's leadership and the invited guests took part.



Tracks and special sessions

The programme covered five technical tracks, a Women in Engineering track and two special sessions led by partner institutions.

1. AI-enabled Computing Techniques
2. IoT Solutions for Sustainable Development
3. Embedded and VLSI Design for Edge Computing
4. Next Generation Communication Networks
5. AI for Signal and Image Processing
6. Women in Engineering
7. Special Session by FICORE, Finland
8. Special Session by UTeM, Malaysia

Keynote speakers

The poster lists twelve keynote speakers from five countries, with Finland best represented.

Speaker	Affiliation	Country
Stephan Sigg	Aalto University	Finland
Lauri Järvilehto	Aalto University	Finland
Hong-Linh Truong	Aalto University	Finland

Speaker	Affiliation	Country
Nandana Rajatheva	University of Oulu	Finland
Bo Tan	Tampere University	Finland
Markku Turunen	Tampere University	Finland
Tomi Salo	University of Vaasa	Finland
Sivakumar S	UTeM	Malaysia
Svetlana Stanarevic	University of Belgrade	Serbia
Simon X. Yang	University of Guelph	Canada
Ajay Lotan Thakur	Intel	Canada
Peter Hofstee	IBM	USA

Sponsors and technical co-sponsors

The poster credits these sponsors and technical co-sponsors:

- SERB (India)
- FICORE (Finnish Indian Consortia for Research and Education)
- IEEE Madras Section
- Digital India
- Aalto University
- UTeM (Universiti Teknikal Malaysia Melaka)
- IEEE Industrial Electronics Society, Madras Section Chapter
- Scopus

VDAT 2024 – 28th IEEE International Symposium on VLSI Design and Test

School of Electronics Engineering, Vellore Institute of Technology (VIT), Vellore · 1–3 September 2024

1. Event at a Glance

Item	Details
Event	28th IEEE International Symposium on VLSI Design and Test (VDAT-2024)
Theme	Emerging Technologies for VLSI Design Ecosystem
Dates	1–3 September 2024 (three-day, in-person)
Tutorials	1 September 2024
Conference	2–3 September 2024
Venue	Vellore Institute of Technology, Vellore, Tamil Nadu, India
Organiser	School of Electronics Engineering (SENSE), VIT Vellore
Supported by	VLSI Society of India (VSI)
Chief Guest	Mr Hitesh Garg, Vice President and India Managing Director, NXP Semiconductors
Visionary Keynote	Mr Sridhar Vembu, Co-Founder and CEO, Zoho Corporation
Guest of Honour	Dr Satya Gupta, President, VLSI Society of India
Publication	IEEE Xplore, conference #63601, DOI 10.1109/VDAT63601.2024
Contact	vdat.chair@vit.ac.in

2. Background

The VLSI Design and Test Symposium (VDAT) began as a workshop in 1998 and became an annual symposium in 2005. It gives academia, researchers, startups and industry practitioners a forum to share ideas, experience and knowledge in VLSI design and testing. The 2024 edition, the 28th, was hosted by VIT Vellore as a three-day in-person event with the support of the VLSI Society of India.

3. Scope and Technical Areas

The call for papers invited highly technical submissions on emerging trends in the following areas. All full-length papers presented at the conference were to be submitted to the IEEE Xplore Digital Library, subject to IEEE quality requirements, and subsequently indexed in Scopus.

- Emerging devices: 2D and advanced material electronics; emerging memory technologies

- VLSI circuit and system design: analog, mixed-signal and RF IC design; digital VLSI architectures; ML-based intelligence in IoT under tight energy and power budgets; secure and intelligent SoC design for automotive, health and defence applications
- CAD for VLSI: logic and behavioural synthesis; floor planning, placement, clock tree synthesis and routing; design automation and methodologies; trusted design automation and tool flow
- Testing and verification: design verification, test, reliability and fault tolerance; formal verification; DFT; fault modelling; pre-silicon design, verification and validation; post-silicon validation; analog, mixed-signal and RF test; functional safety and test methods

The programme also included tutorials (half-day and full-day), a design contest, a PhD research forum, and an industry exhibition.

4. Distinguished Guests

- Chief Guest: Mr Hitesh Garg, Vice President and India Managing Director, NXP Semiconductors
- Visionary Keynote Speaker: Mr Sridhar Vembu, Co-Founder and CEO, Zoho Corporation
- Guest of Honour: Dr Satya Gupta, President, VLSI Society of India



Fig. 1. Ceremonial sapling watering by guests at the venue entrance (name board: Dr Satya Gupta, VLSI Society of India).



Fig. 2. Ceremonial sapling watering (name board: Shri Hitesh Garg, NXP India).

5. Speakers and Panelists

The symposium website lists 39 speakers and panelists from industry, research institutes and academia.

Organisation	Speakers
NXP Semiconductors	Hitesh Garg; Preet Yadav (India Innovation Ecosystem, panel)
Zoho Corporation	Sridhar Vembu
VLSI Society of India	Satya Gupta; Chitra Hariharan
Marvell	Navin Bishnoi; Aquib Quraishi; Aanand Venkatachalam; Suraj MC

Cadence	Lalit Mohan; Sachin Shrivastava; Vishal Rastogi; Deepak Karnatak
Synopsys	Shamitha Rao
Siemens EDA	Srijesh Parambath
Microchip	Dr Renold Sam; Yadu Krishnan
C-DAC	Dr S.D. Sudarsan (Bangalore); Venkata Reddy Kolagatla; Shramona Roy; Vivian Desalphine
Renesas Electronics India	Nachiket Hardas
Yokogawa Solution Service Corporation	Mickael Lozac'h
Mirafra	Alok Kuchlous
VLSIMONKS Design	Vijay Kanth; Mohan Ganugapati
ChipEdge Technologies	Sreedevi Kulkarni; Venkat Sunkara
Maven Silicon	Putta Satish
Dissai Technologies	Dr Dhayalakumar M
Enthu Technology Solutions	Dr Subramanian
OlaKrutrim	Srikanth Puvvada
IIT Roorkee	Prof. Sudeb Dasgupta
IIT Bhubaneswar	Prof. Navjeet Bagga
IIIT Bangalore	Sakshi Arora
NIT Tiruchirappalli	Manikandan R R
IIITDM Kancheepuram	Dr Noor Mohammed
VNIT	Ganesh C. Patil
VIT	Dr Kanchana Bhaaskaran, Vice Chancellor



Fig. 3. Ceremonial sapling watering (name board: Shri Navin Bishnoi, Marvell India).



Fig. 4. A speaker addressing the delegates at the VDAT 2024 podium.

6. Tutorials, Design Contest and PhD Forum

Tutorials were held on 1 September 2024, ahead of the main conference on 2–3 September. The organisers invited half-day (3 hour) and full-day (6 hour) tutorial proposals that carry continuing educational value and focus on generic or advanced concepts rather than company marketing

material. The event also featured a design contest and a PhD research forum, and delegates could visit industry exhibit booths.

7. Awards

Best Paper: "Design and Simulation of Class-E Power Amplifier for 13.56 MHz Near Field Communication Technology Applications" by Ganesh Racha, K Lal Kishore, Yedukondalu Kamatham and P Srinivasa Rao, CVR College of Engineering, Hyderabad.

Design Contest Winners

Position	Prize	Title	Team	Affiliation
1st	₹15,000	LoRaWAN IoT Cloud System for Irrigation	Ishan Urgaonkar, Arya Sadanand Patil	VIT Vellore
2nd	₹10,000	Face Video-Based Vital Signs Detection	Devesh Shevde	VIT Vellore

8. Publication and Outcome

The proceedings of VDAT-2024 are published in IEEE Xplore. The VDAT team thanked the guests, sponsors, keynote and tutorial speakers, session chairs, exhibitors, industry and academia delegates, students, VIT management, faculty and staff for their contribution to the success of the 28th edition.

9. About the Organisers

VIT was established in 1984 and became a deemed university in 2001, with campuses at Vellore, Chennai, Bhopal and Amaravati.

School of Electronics Engineering (SENSE) offers 3 undergraduate programmes, 6 postgraduate programmes (including M.Tech in VLSI Design and Embedded Systems) and 2 PhD routes, including the recently introduced B.Tech in Electronics Engineering with a VLSI Technology specialisation. The school reports 226 faculty, over 3,000 UG students, 448 PG students, over 200 PhD scholars, 3,000+ journal publications, 17 industry consultancies, ₹10 crore in sponsored projects and 22 granted patents.

Industry Academia Conclave 2024: Next Generation Communication'24

School of Electronics Engineering, Vellore Institute of Technology (VIT) · 13 September 2024

1. Event at a Glance

Item	Details
Event type	Industry Academia Conclave (5th edition)
Title	Next Generation Communication'24
Targeted SDGs	SDG 4: Quality Education; SDG 9: Industry, Innovation and Infrastructure
Date	13 September 2024 (Friday)
Time	9:30 AM – 4:30 PM
Venues	Ambedkar Auditorium, TT727 and TT312
Participants	320
Chief Guest	Mrs Vijai Ekambaram, Digital Strategy and Transformation Leader – Network Systems, Verizon Data Services, Chennai
Coordinators	Dr S. Sivanantham (Micro and Nano Electronics), Dr Noor Mohammed V (Communication Engineering), Dr N. Rajesh (Communication Engineering)

2. Introduction

The fifth Industry Academia Conclave, themed Next Generation Communication, was organised by the School of Electronics Engineering, VIT, on 13 September 2024. The conclave brought together industry experts from companies such as Verizon, Samsung R&D, Nokia, Ericsson, Cisco, Synopsys, L&T Technology Services, ABB, Magna International and VVDN Technologies to interact with M.Tech students and faculty. Twelve speakers presented across four sessions running in parallel at three venues, covering 5G, 6G, AI in networking, memory interfaces, automotive electronics and industry-ready skills.

3. Organising Committee

- Chief Patron: Dr G. Viswanathan, Chancellor
- Patrons: Shri Shankar Viswanathan, Dr Sekar Viswanathan and Dr G.V. Selvam (Vice Presidents); Dr V. Kanchana Bhaaskaran (Vice Chancellor); Dr Partha Sarathi Mallick (Pro Vice Chancellor); Dr T. Jayabharathi (Registrar)
- Convener: Dr S. Sivanantham, Dean, School of Electronics Engineering
- Co-Convener: Dr N. Rajesh, Assistant Professor, DCE

- Coordinators: Dr K. Vinoth Babu, Dr R.K. Mugelan, Dr A. Karthikeyan, Dr Muthuraja, Dr Jagana Bihari Pathy, Dr Naveen Mishra, Dr K.K. Abdul Majeed, Dr Kishor Lakshmi Narayanan
- Advisory Committee: Dr B. Karthikeyan (HOD/DET), Dr Jagannadha Naidu (HOD/DMNE), Dr Noor Mohammed V (HOD/DCE), Dr Vidhya S (HOD/DSBT)

4. Programme Schedule

Time	Programme
9:30 – 10:30 AM	Inauguration (Ambedkar Auditorium)
10:30 – 10:45 AM	Tea break
11:00 AM – 12:00 Noon	Session 1
12:10 – 1:15 PM	Session 2
1:00 – 2:00 PM	Lunch
2:00 – 3:00 PM	Session 3
3:00 – 3:15 PM	Tea break
3:15 – 4:15 PM	Session 4

5. Inauguration

The inauguration was held at the Ambedkar Auditorium at 9:30 AM. The Associate Dean welcomed the gathering and delivered the inaugural talk. Mrs Vijai Ekambaram of Verizon, the Chief Guest, delivered the address, and Dr Noor Mohammed, HOD/CE, proposed the vote of thanks. M.Tech students and faculty members attended.

6. Technical Sessions

Session	Speaker	Topic	Venue
1	Mrs Vijai Ekambaram (Verizon)	5G Hits and Misses	Ambedkar Auditorium
1	Dr Serene Banerjee (Ericsson)	Causal AI for 6G	TT727
1	Mr Vignesh RS (Cisco)	The Future of Network: AI Powered Networking Solutions	TT312
2	Mr Rahul Saxena (Synopsys)	Overview and Importance of Logic Libraries	Ambedkar Auditorium
2	Mr Subhash Kumar (ABB)	TSN as a Way Forward for IT-OT Convergence	TT727
2	Mr Sudheer Kumar H U and Dr Satya Kumar Vankayala (Samsung R&D)	AI and ML for Wireless Networks	TT312
3	Mr Dinesh Patil (Synopsys)	Memory Interfaces – Powering Era of AI	Ambedkar Auditorium
3	Dr Vishnu Vardhan Gudla (L&T Technology Services)	Opportunities and Challenges of OTFS Modulation for 6G	TT727
3	Dr Vetrivel Chezian (Nokia)	Pushing the Boundaries: Physical Layer Challenges	TT312

		in 6G	
4	Mr Tetala Neelkanth Reddy (VVDN Technologies)	From Classroom Concepts to Industry Applications: Essential Electronics Engineering Skills	Ambedkar Auditorium
4	Mr Jayaram Choudhury and Mr Kiran Rajappanavar (Magna International)	ADAS in Automotive System	TT727

6.1 Session Summaries

AI-powered networking and telecom (TT312). Mr Vignesh RS discussed the challenges and considerations of embedding AI into networking, including fully autonomous networks, integration with IoT and smart devices, AI-enhanced network slicing and AI for improved user experience. Mr Sudheer Kumar of Samsung, Bangalore, spoke on AI/ML in telecom networks, covering the key benefits of AI in telecom, 5G SA and 5G Core, NWDAF, MDAS and AI in RAN. Dr Satya Kumar Vankayala of Samsung Research Institute – India, Bangalore, delivered the second half on ML for 5G wireless systems, covering LLR computation using sparse neural networks, the need for neural networks for LLR, and various simulation parameters.

6G physical layer. Dr Vetrivel Chezian of Nokia presented an overview of cellular technologies and their PHY enablers, then discussed upcoming 6G technologies, near-field communications and holographic communications.

5G Hits and Misses. Mrs Vijai Ekambaram discussed the advantages and disadvantages of 5G, including coverage, indoor service, security, privacy, capacity and regulatory hurdles. The session was highly interactive: the audience cleared many doubts and asked about opportunities for PG students in this field. The speaker was felicitated with a memento by Prof. Valarmathi J.

Memory interfaces and logic libraries. Prof. Abdul Majeed K K introduced Mr Dinesh Patil and Mr Rahul Saxena to the audience. Mr Dinesh Patil briefly introduced Synopsys and its recruitment process and ongoing work, then presented "Memory Interfaces – Powering Era of AI" for about 45 minutes, covering DDR, LPDDR, HBM, GDDR and non-volatile memory interfaces and their role in AI workloads.

Industry-ready skills. Mr Tetala Neelkanth Reddy of VVDN Technologies, Chennai, spoke on moving from classroom concepts to industry applications, stressing the essential skills that bridge theoretical knowledge with practical implementation. He was felicitated with a memento by Prof. Rajeev Pankaj Nelapati.

6.2 Event Photographs



Fig. 1. Mrs Vijai Ekambaram (Chief Guest) addressing the participants.



Fig. 2. Students, faculty and guests attending the session.



Fig. 3. "5G – Hits and Misses" session.

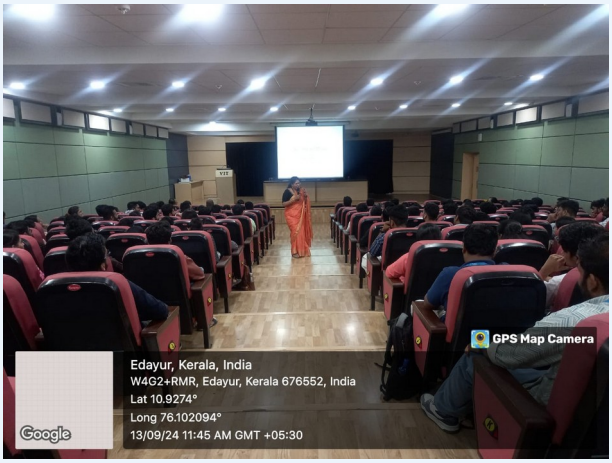
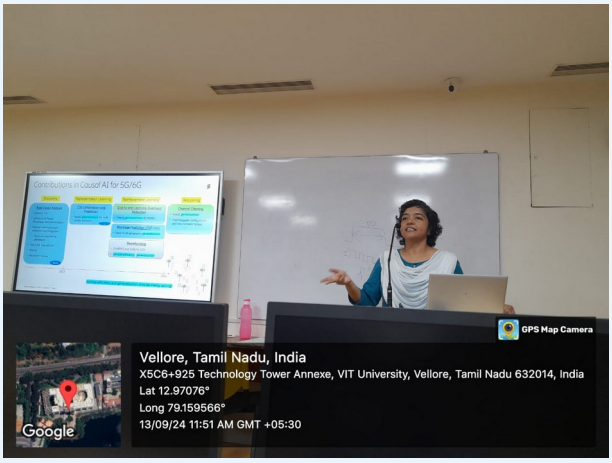


Fig. 4. Interactive discussion during the 5G session.



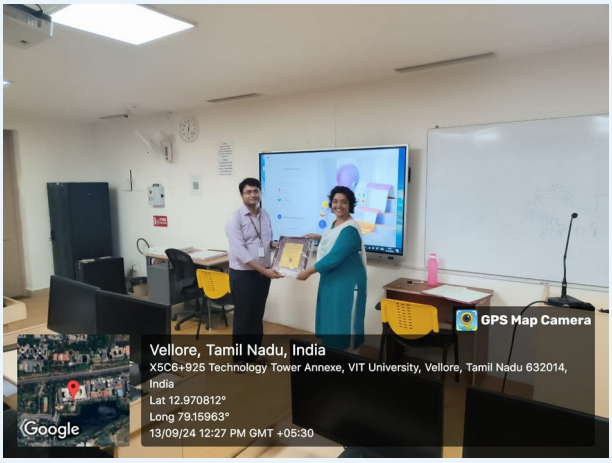


Fig. 5. Dr Serene Banerjee (Ericsson) presenting on Causal AI for 6G at TT727.

Fig. 6. Felicitation of the speaker with a memento at TT727.



Fig. 7. Participants attending the technical session on memory interfaces.



Fig. 8. Mr Dinesh Patil (Synopsys) presenting "Powering the Era of Pervasive Intelligence".

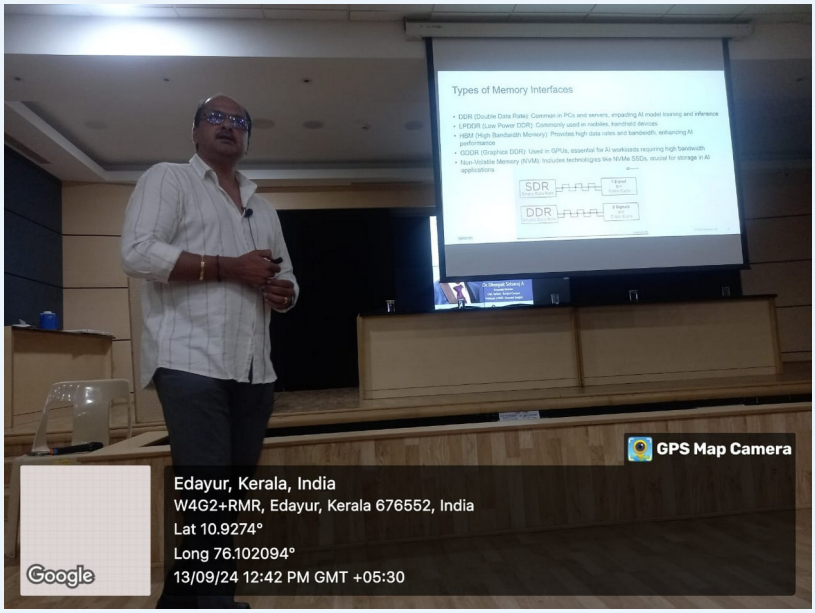


Fig. 9. Mr Dinesh Patil explaining the types of memory interfaces (DDR, LPDDR, HBM, GDDR and non-volatile memory).

7. MoUs Signed with Industry Partners

7.1 MoU with Nokia Solutions and Networks India Pvt. Ltd.

VIT signed a Memorandum of Understanding with Nokia Solutions and Networks India Pvt. Ltd. to pursue 5G and next-generation collaborative research with Artificial Intelligence (AI) and Machine Learning applications. The MoU was signed on 24 June 2024.

- Signed by Dr T. Jayabharathi, VIT Registrar, and Ms Ponni, Director (R&D) and Nokia Bangalore University Collaboration Lead.
- Present: VIT Founder-Chancellor Dr G. Viswanathan; Vice Presidents Mr Sankar Viswanathan and Dr G.V. Selvam; Vice-Chancellor Dr V. S. Kanchana Bhaaskaran; Pro-Vice Chancellor Dr Partha Sharathi Mallick; Dean, School of Electronics Engineering, Dr S. Sivanantham; and Ms Meenakshi S, Leader of Nokia Labs.
- Experts from Nokia will be part of VIT's Board of Studies, mentor students and faculty through hands-on learning, prototyping and student projects, and engage with the relevant VIT departments, linked to the project and skill requirements of Nokia.

7.2 MoU with Marvell India Private Limited

VIT signed a Memorandum of Understanding with Marvell India Private Limited, a global semiconductor solutions company, to strengthen semiconductor education and create career pathways for VIT's postgraduate students. The MoU was exchanged by Dr G. Viswanathan, Founder and Chancellor, VIT, and Mr Navin Bishnoi, India Country Manager and Associate Vice President of Central Engineering, Marvell.

- Marvell delegation: Ms Sandhini Devy, Mr Anoob Joseph, Mr Vinay B., Mr Umesh Kumar Shukla and Ms Radharani Danda.
- VIT: Dr Sekar Viswanathan (Vice President), Dr Sandhya Pentareddy (Executive Director), Dr Kanchana Bhaaskaran (Vice Chancellor), Dr Partha Sharathi Mallick (Pro-Vice Chancellor), Dr Samuel Rajkumar (Director, CDC), Dr Sivanantham S (Director, VSPACE Centre), Dr Jasmin Pemeena (Dean, SENSE) and Dr Jayakrishnan P (Assistant Director, CDC).
- Academic and technical workshops: joint guest lectures, seminars and skill-based professional development programmes.
- Internships: hands-on industry experience at Marvell for eligible VIT postgraduate students.
- Flexible delivery: hybrid learning modules combining virtual sessions and in-person instruction.

Note: VIT's announcement of the Marvell MoU does not state the signing date; it was published on 28 August 2026, so this MoU post-dates the September 2024 conclave.

8. Expenditure

S.No	Component	Expenditure (₹)	Source
1	Mementos – 13 nos	15,600	School Budget
2	Refreshments – participants (FN: 320, AN: 300)	21,700	School Budget
3	Refreshments – guests (40 nos)	240	School Budget
	Total	37,540	

9. Attendance

The attendance sheets of the participating M.Tech students and the session-wise sheets (including the TAC-2024 sheet at TT727) are enclosed with the original event file. Recorded participation was 320.

10. Outcome

The conclave exposed postgraduate students to current industry work in 5G/6G, AI-enabled networks, EDA and memory interfaces, automotive electronics and employability skills, and gave faculty a channel to industry for curriculum and project collaboration. It supports SDG 4 (Quality Education) and SDG 9 (Industry, Innovation and Infrastructure).

EMERGENT TRENDS & TECHNOLOGY

- UPCOMING TECHNOLOGIES

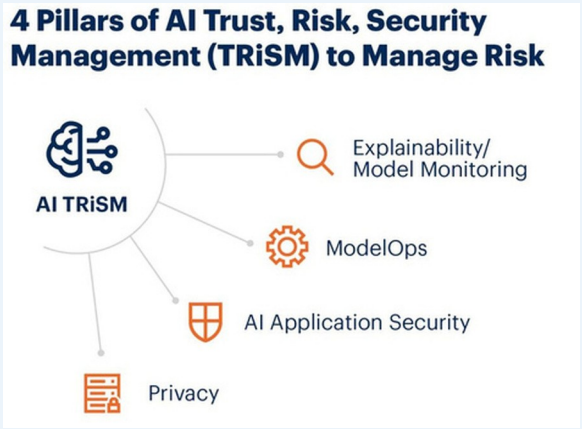
AI TRiSM and Quantum Security



Dr. Debashish Dash
Assistant Professor, SENSE
Department of Micro and Nano Technology

AI TRiSM (Artificial Intelligence Trust, Risk and Security Management) and Quantum Security are two emerging technology domains that address the reliability, safety, privacy, and security of next-generation intelligent systems. They can be integrated into a promising research area combining Trustworthy AI, Cybersecurity, Quantum Computing, and Post-Quantum Cryptography. AI TRiSM focuses on ensuring that AI systems are trustworthy, secure, transparent, reliable, and compliant.





AI TRiSM, or artificial intelligence (AI) trust, risk and security management (AI TRiSM), "ensures AI model governance, trustworthiness, fairness, reliability, robustness, efficacy and data protection. This includes solutions and techniques for model interpretability and explainability, AI data protection, model operations and adversarial attack resistance." While numerous, separate frameworks focus specifically on AI trust, AI risk or AI security, they're challenging to integrate and synchronize, according to researchers. This lack of coordination can result in fragmented AI management. It can also lead to knowledge gaps in the risks and security consequences stemming from AI implementation and AI practices. The AI TRiSM framework, however, provides a unified approach. It brings together the important parts of different frameworks for more comprehensive management of AI technologies.

AI TRiSM and Quantum Security complement each other. Pictorially, they can be shown:





In summary, global standards (such as NIST and CNSA 2.0 guidelines) mandate that governments and critical infrastructure transition to quantum-resistant algorithms by 2030–2035 to prevent a collapse of modern digital trust.

Emerging Trends in VLSI 2024



Dr. Sivanantham S
Professor, SENSE
Department of Micro & Nano Engineering

VLSI technology is rapidly evolving in 2024, driven by advancements that focus on making microchips faster, more efficient, and smaller. Key trends include the rise of 2nm and 3nm chip technology, enhancing chip density and reducing power consumption for high-performance devices. AI and machine learning integration into VLSI design is improving automated testing and optimization processes. 3D integrated circuits are becoming more prominent, allowing for better chip stacking and reduced latency. Additionally, RISC-V architecture is gaining traction, offering an open-source alternative for chip designers. These innovations are propelling VLSI to meet the growing demands of modern technologies like IoT, AI, and 5G.

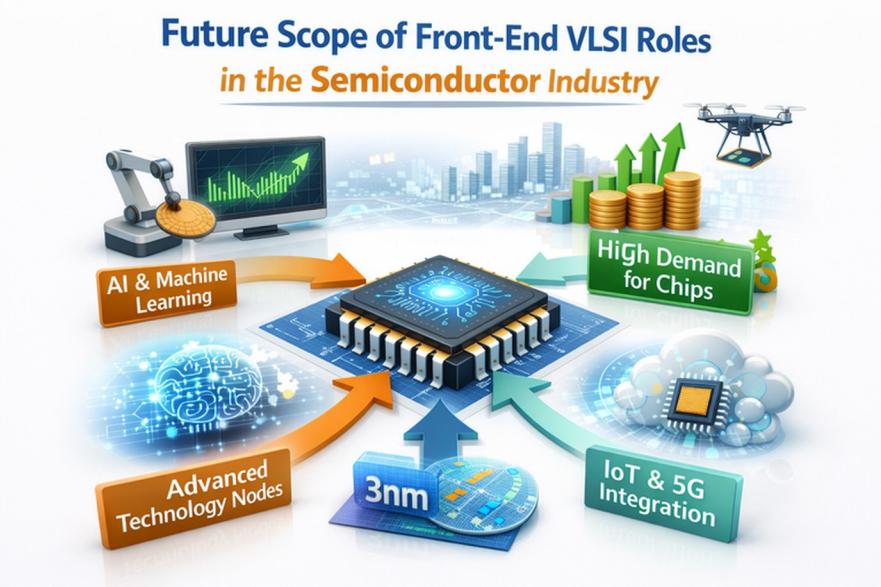
Key Trends

2nm and 3nm Chip Technology. The push for smaller and faster chips continues, with leading manufacturers like TSMC and Intel developing 2nm and 3nm chip processes. These smaller nodes help create more compact, power-efficient devices, which are essential for advanced applications like AI, mobile computing, and IoT.

3D Integrated Circuits (3D ICs). 3D IC technology allows the stacking of multiple layers of silicon wafers, reducing the physical space required while boosting performance. For example, AMD uses 3D stacking in its latest processors to enhance data transfer rates and minimize latency.

RISC-V Architecture. The RISC-V open-source architecture is gaining traction as a cost-effective alternative for chip designers, encouraging innovation. Companies like NVIDIA and Western Digital are exploring RISC-V for more customizable solutions.

AI Integration in VLSI Design. AI is transforming the VLSI design process by automating layout generation, verification, and testing. Machine learning models help predict potential errors, reducing manual intervention and speeding up chip design cycles.



The future of VLSI (Very Large Scale Integration) is promising, with continuous advancements focusing on smaller, faster, and more power-efficient chips. Emerging trends like 2nm and 3nm chip nodes, 3D ICs, and AI-driven design processes are transforming VLSI's role in cutting-edge technologies, from AI and IoT to autonomous vehicles. This evolution offers vast opportunities for aspiring VLSI engineers.

A career in VLSI can be highly rewarding, given the growing demand for skilled professionals in sectors like semiconductor manufacturing, consumer electronics, and automotive. Learning VLSI technology provides a foundation for roles such as chip design engineer, verification engineer, and circuit analyst.

The emerging trends in VLSI technology for 2024 are set to reshape the future of electronics by focusing on miniaturization, power efficiency, and higher integration. Innovations such as 2nm chip technology, 3D ICs, AI integration, and RISC-V architecture are pushing the boundaries of what is possible in microchip design, enabling smarter and more efficient devices. These advancements are essential to meet the increasing demands for speed, performance, and compactness in applications ranging from IoT to high-performance computing. By keeping up with these trends, VLSI engineers and professionals can contribute to driving technological growth in a dynamic industry.

Reconfigurable Intelligent Surfaces: Transforming Wireless Communication Towards 6G Networks



Dr. Hemanta Kumar Sahu
Assistant Professor
Department of Communication Engineering
School of Electronics Engineering (SENSE)

The rapid evolution of wireless communication has created an increasing demand for high data rates, seamless connectivity, improved spectral efficiency, and energy-efficient network architectures. While fifth-generation (5G) communication has significantly enhanced mobile connectivity, the growing requirements of emerging applications are driving research towards sixth-generation (6G) wireless networks. Among the promising technologies envisioned for 6G, Reconfigurable Intelligent Surfaces (RIS) have emerged as an innovative approach to transforming the wireless propagation environment.

RIS is a programmable surface comprising a large number of low-cost electromagnetic reflecting elements, each capable of controlling the phase and, in some architectures, the amplitude of incident electromagnetic waves. By intelligently adjusting these elements, RIS can redirect wireless signals towards intended receivers, enhance signal strength, mitigate coverage limitations, and improve communication reliability. Unlike conventional wireless systems, which adapt to the propagation environment, RIS enables the wireless environment itself to be intelligently controlled. Figure 1 shows a typical RIS-assisted link: a controller configures the surface so that the reflected path through the RIS (hA,n followed by hB,n) combines with the direct path (hd) at the receiver.

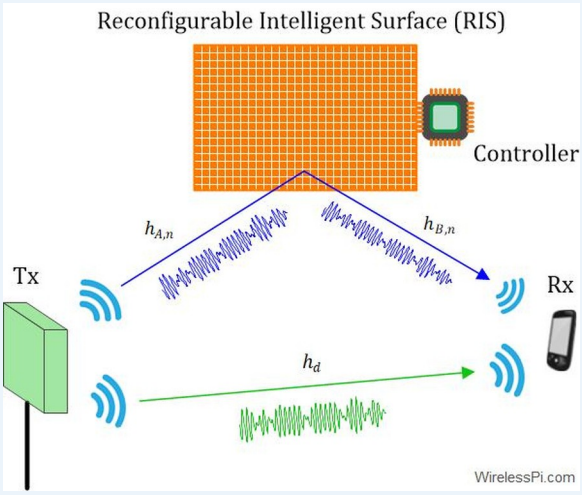


Figure 1: Structure of a RIS-assisted link, showing the controller, the direct channel (hd) and the reflected channels (hA,n and hB,n). Source: WirelessPi.com

A practical benefit of RIS is coverage extension in dense urban areas. As Figure 2 shows, when a building blocks the line-of-sight (LOS) link between a base station (BS) and a user (UE 2), an intelligent reflecting surface (IRS) mounted on a nearby building can create a controllable reflected path that restores the connection. Meanwhile, UE 1 continues to be served over its direct LOS link. In this way, RIS fills coverage gaps without adding a new base station.

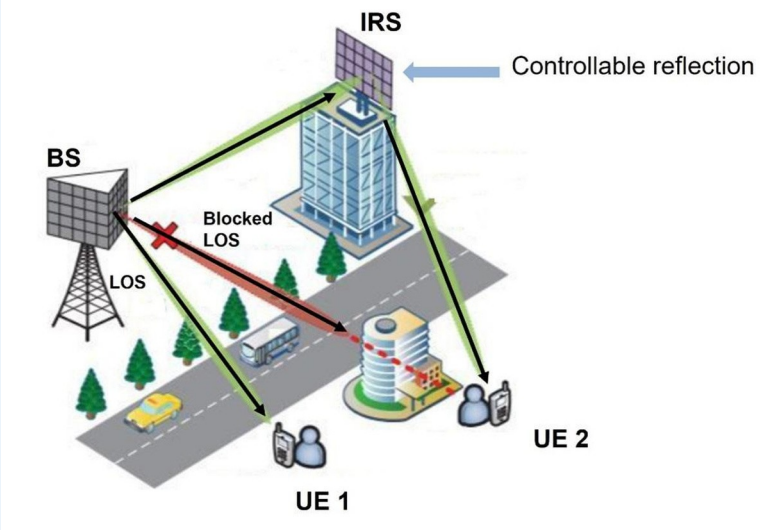


Figure 2: An IRS restoring coverage to a user (UE 2) whose LOS link to the base station is blocked.

A significant research advancement in this area is the development of active and passive RIS architectures. Passive RIS operates by reflecting incident signals without requiring additional amplification, offering low power consumption and relatively simple implementation. However, its performance can be limited by propagation losses and the multiplicative fading effect associated with cascaded wireless channels. Active RIS addresses some of these limitations by incorporating amplification capabilities into the reflecting elements, thereby improving received signal strength.

Nevertheless, the additional amplification introduces hardware complexity, power consumption, and amplified noise, creating important design trade-offs for practical deployment.

Another promising research direction is the integration of RIS with cooperative relaying systems. In such configurations, an intermediate relay assists communication between a source and destination, while intelligently configured RIS elements enhance the individual communication links. Combining active and passive RIS with amplify-and-forward (AF) or decode-and-forward (DF) relaying can potentially improve coverage, transmission reliability, and network performance. The investigation of heterogeneous fading environments, including Rayleigh and Rician channels, is particularly important for understanding the performance of these systems under realistic wireless propagation conditions.

Despite their potential, RIS-assisted wireless networks face several research challenges. Accurate channel estimation, optimal phase-shift configuration, hardware impairments, amplification noise, energy efficiency, and the practical deployment of large-scale intelligent surfaces remain important considerations. Furthermore, analytical performance evaluation using metrics such as outage probability, average bit error probability, and achievable data rate is essential for understanding system behaviour and developing reliable network designs.

Looking ahead, RIS technology is expected to play an important role in shaping intelligent and adaptive 6G communication networks. Its integration with cooperative relaying, advanced signal processing, and emerging network architectures offers exciting opportunities for future research. Continued investigations into practical RIS configurations, realistic channel models, and energy-efficient transmission strategies will be crucial to bridging the gap between theoretical developments and real-world implementation. RIS therefore represents not merely an advancement in antenna technology, but a paradigm shift towards programmable wireless environments and intelligent connectivity.

AUGMENTED & VIRTUAL REALITY

Extended Reality: Technology, Construction and Applications

Dr A Sangeetha, Associate Professor, School of Electronics Engineering, Vellore Institute of Technology

A concise technology feature on AR, VR and mixed reality



Figure 1. An original illustration of an immersive mixed-reality workspace.

1. Introduction

Extended Reality (XR) is an umbrella term for technologies that combine digital content with human perception. It includes Augmented Reality (AR), Virtual Reality (VR) and Mixed Reality (MR). VR immerses the user in a computer-generated environment, replacing the view of the physical world. AR places digital information—such as images, labels or 3D objects—over the user's view of the real environment. MR connects digital objects to physical surroundings so that they appear to occupy and respond to the real space. In 2024, XR moved further into the commercial market, with premium mixed-reality headsets, lower-cost devices and new platform initiatives competing for users and developers.

2. Technology

AR and VR systems combine display technology, sensing, computing and software. Head-mounted displays use screens and optical elements to present images to the eyes. Cameras and motion sensors collect information about the user and the surrounding environment. Tracking systems estimate head position and orientation; some devices also track eye gaze and hand movements. A processor, often supported by a graphics-processing unit, interprets sensor data and renders the virtual scene. Software platforms and development tools provide the operating environment and applications. In passthrough mixed-reality headsets, outward-facing cameras capture the real world and the internal displays show that camera view together with digital objects. Optical see-through AR glasses instead allow the user to look through transparent lenses.

3. Construction

A typical XR headset is constructed from several integrated assemblies. The outer housing and adjustable head strap support the device and help position it comfortably. Inside the front enclosure are one or more display panels, lenses or optical waveguides, and the electronics required to drive the displays. Cameras and other sensors are placed around the headset to observe the environment and measure movement. A processor board handles sensor input, tracking and graphics; power-management electronics and a rechargeable battery supply energy. Speakers or spatial-audio components provide sound, while microphones support voice input. Depending on the device, additional components may include eye-tracking cameras, hand-tracking sensors and controllers. The hardware is coordinated by system software, tracking algorithms and an XR application platform. The precise arrangement varies between VR headsets, passthrough MR headsets and transparent-lens AR glasses.

4. Working Principle

XR operation follows a continuous sense–process–render–display cycle. First, cameras and motion sensors capture the user's surroundings and movements. The system estimates the position and orientation of the head, and—where supported—the location of the eyes or hands. Next, the processor combines this information with the application data to determine what should appear from the user's current viewpoint. The graphics system renders a perspective-correct image, usually generating a separate view for each eye to create depth. The displays then present the images through lenses or optical elements. This cycle repeats many times per second so that the virtual scene updates as the user moves. The 2024 article notes refresh modes of 90, 96 and 100 Hz for Apple Vision Pro and explains that excessive delay between movement and visual updating can disrupt immersion and cause discomfort. In AR, digital elements are aligned with the real-world view; in VR, the headset presents a predominantly computer-generated environment.

5. Applications

AR and VR can support activities in which visual guidance, spatial understanding or realistic simulation is useful. In education and training, immersive environments can help learners explore three-dimensional subjects and practise procedures in simulated settings. In healthcare, 3D visualisation and simulation can support medical education and the planning or rehearsal of selected procedures. In manufacturing, engineering and maintenance, AR overlays can present instructions or contextual information while VR can be used to practise tasks without occupying physical equipment. Architecture and real estate can use immersive walkthroughs to communicate building designs and interior layouts. Retail applications can let customers preview products or furnishings in a space. Tourism and cultural organisations can provide virtual visits and contextual information at places of interest. Gaming and entertainment remain prominent uses of VR, while collaborative virtual workspaces offer ways to meet and interact with shared digital content. These are representative application areas; the 2024 source specifically highlights commercial growth and increased demand in education.

6. Limitations

Despite rapid development, AR and VR continue to face practical and technical limitations. Cost remains a barrier: premium headsets can be expensive, while lower-priced models may compromise on display resolution or optical quality. Comfort and power are also important challenges. Headsets add weight to the face and batteries generally last hours rather than days; the 2024 article cites approximately 2.5 hours for Meta Quest 3S. Visual limitations include restricted field of view, display brightness and difficulty making transparent-lens AR glasses look like ordinary eyewear. Tracking errors or delays can reduce the stability of virtual objects, and latency may contribute to discomfort or motion sickness. Cameras and sensors also raise questions about privacy because they may collect information about users and their surroundings. Finally, the usefulness of XR depends on the availability of compelling applications and content. Wider adoption will depend on making devices lighter, more affordable, more comfortable and more useful in everyday settings.



Figure 2. Original visual overview of XR concepts and representative device/application areas. The image is illustrative; the written sections provide the authoritative explanation.

TECHNOLOGY FEATURE • AUTONOMOUS SYSTEMS

Autonomous Systems Beyond Roads: Unmanned Aerial and Underwater Vehicles

Dr A Sangeetha, Associate Professor, School of Electronics Engineering, Vellore Institute of Technology

From three-dimensional airspace to the ocean depths, intelligent machines are executing complex industrial, scientific, and defense missions where direct human control is impractical.

1. Introduction

As autonomous systems expand beyond terrestrial transport, Unmanned Aerial Vehicles (UAVs) and Unmanned Underwater Vehicles (UUVs) have emerged as transformative platforms engineered for environments where continuous human oversight is hazardous, costly, or physically impossible (Autonomous Robots and Vehicles Magazine, 2026). While autonomous road transport centers on robotaxis navigating mapped urban roadways, aerial and subsea platforms extend machine intelligence into open airspace and deep-sea waters.

Rather than merely repeating pre-programmed sequences, modern aerial and underwater vehicles sense dynamic surroundings, interpret changing environmental conditions, plan safe trajectories, and verify mission outcomes in real time.

2. Technology

Contemporary UAVs and UUVs rely on multi-layered technological architectures that combine specialized environmental sensors with edge-computed artificial intelligence (Autonomous Robots and Vehicles Magazine, 2026):

Domain-Specific Sensor Integration: Aerial platforms fuse Global Navigation Satellite Systems (GNSS), high-resolution optical cameras, LiDAR, millimeter-wave radar, and Inertial Measurement Units (IMUs) to maintain spatial awareness. Because radio frequencies and satellite signals attenuate rapidly in water, underwater platforms substitute GPS with acoustic positioning, Doppler Velocity Logs (DVLs), and multi-beam sonar arrays.

Perception and Artificial Intelligence: Onboard perception pipelines detect, classify, and track obstacles in real time. Emerging end-to-end learning models and vision-language-action architectures enable machines to interpret high-level mission objectives, reason about unfamiliar surroundings, and generate precise physical control commands.

Adaptive Decision-Making: Moving beyond rigid waypoint scripts, autonomous flight and dive controllers continuously evaluate dynamic external forces—such as atmospheric wind shear or subsurface ocean currents—to recalculate energy-efficient, collision-free paths independently.

3. Construction

Unmanned Aerial Vehicles (UAVs)



Figure 1. Autonomous Delivery UAV: Multirotor composite airframe equipped with top-mounted LiDAR, dual GNSS antennas, forward optical and radar detect-and-avoid sensors, and an underslung medical payload module operating along an automated corridor from a central logistics hub.

Airframe and Propulsion: Constructed as multirotor or fixed-wing frames using high-strength, lightweight carbon-fiber composites to maximize aerodynamic efficiency, structural rigidity, and useful payload ratio.

Payload Systems: Engineered with weather-sealed internal bays or precision-latched underslung compartments designed to secure medical supplies, commercial parcels, or high-resolution inspection cameras.

Onboard Electronics: Integrates hardened flight-control processors, redundant battery-management units, encrypted telemetry transceivers, and multi-directional sensor pods for 360-degree hazard detection.

Unmanned Underwater Vehicles (UUVs)

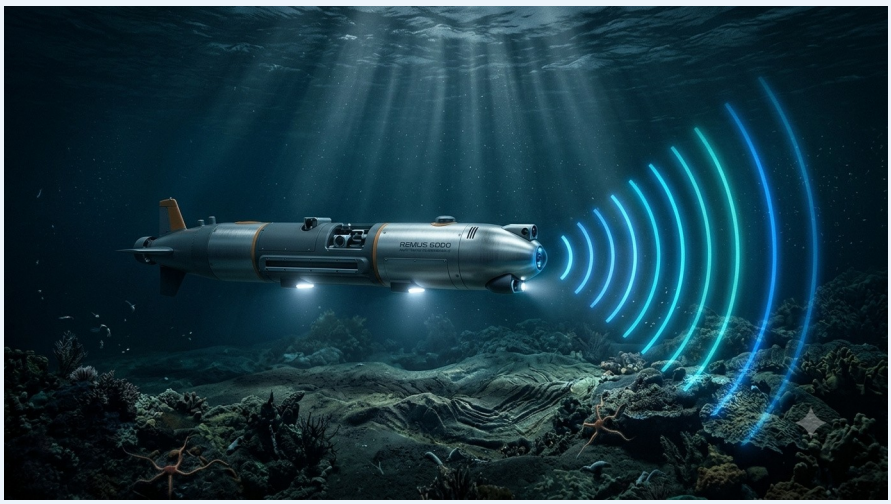


Figure 2. Autonomous Underwater Vehicle (UUV): Hydrodynamic modular pressure hull projecting forward acoustic sonar waves across the seabed, integrating watertight navigation electronics, a mid-body payload bay, and a rear thruster propulsion assembly.

Hydrodynamic Pressure Hull: Built with streamlined, torpedo-shaped modular shells fabricated from marine-grade aluminum, titanium, or syntactic foam composites to resist extreme hydrostatic pressure while minimizing drag.

Acoustic and Navigation Suites: Houses bow-mounted sonar transducers, acoustic modems, optical spotlights, and watertight Inertial Navigation Systems (INS) capable of operating without surface links.

Modular Payload Bays: Features configurable mid-body sections that accept interchangeable oceanographic sensors, bathymetric multi-beam sonars, high-definition subsea cameras, or specialized defense instruments.

4. Working Principle

Although both vehicle classes execute a continuous sense–decide–act feedback loop, their operational physics differ sharply between air and water:

Operational Stage	Unmanned Aerial Vehicles (UAVs)	Unmanned Underwater Vehicles (UUVs)
Localization & Navigation	Combines satellite GNSS fixes with IMU data and visual odometry to maintain centimeter-level 3D positioning along pre-approved aerial corridors (FAA, 2026).	Relies on dead reckoning—fusing high-precision INS gyroscopes with bottom-tracking Doppler Velocity Logs (DVLs) and periodic acoustic beacons—since GPS cannot penetrate water (Defense and Marine Research Institute, 2026).
Hazard Detection	Executes a detect, navigate, avoid, and deliver loop using forward radar,	Emits active forward-looking and side-scan acoustic sonar pulses,

	LiDAR, and stereo cameras to identify birds, aircraft, power lines, and terrain.	analyzing returning echoes to map seabed topography and steer clear of reefs, wrecks, or subsea cables.
Mission Execution & Recovery	Adjusts rotor thrust in real time to stabilize hover, lowers or releases cargo at verified drop zones, and returns autonomously to a charging hub.	Follows lawnmower survey grids autonomously for days or weeks, surfacing at scheduled waypoints to transmit data or rendezvous at a recovery vessel.

5. Applications

Aerial Applications (UAVs): Automated inspection of high-voltage transmission lines, wind turbines, and pipelines; multispectral crop mapping in precision agriculture; rapid delivery of blood products, vaccines, and emergency medical kits; and post-disaster search-and-rescue mapping (Autonomous Robots and Vehicles Magazine, 2026).

Underwater Applications (UUVs): Integrity inspection of offshore wind foundations, subsea telecommunications cables, and oil-and-gas pipelines; high-resolution bathymetric seabed charting; long-duration oceanographic and climate monitoring; and naval mine countermeasures and harbor security (Defense and Marine Research Institute, 2026).

6. Limitations

UAV Constraints: Commercial scaling remains governed by strict aviation regulations—particularly Beyond Visual Line of Sight (BVLOS) airspace rules—alongside finite lithium-battery energy density that limits flight endurance, sensitivity to high winds and precipitation, and rigorous safety certification standards for automated detect-and-avoid systems (FAA, 2026).

UUV Constraints: Subsea operations face severe acoustic communication bandwidth limits and high signal latency that preclude real-time human teleoperation, extreme hydrostatic pressure and saltwater corrosion demands, finite onboard energy storage for multi-week missions, and complex open-ocean launch and recovery logistics (Defense and Marine Research Institute, 2026).

References

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Alumni Spotlight



Shantanu Anand
Data Analytics Senior Consultant
Deloitte USI, McKinsey Forward 25
Hyderabad, Telangana, India
Batch of 2024

As an Analytics Specialist Consultant within Deloitte USI's Audit and Assurance practice, I work across industries including Consumer, Life Sciences, Healthcare, and more enabling audit teams to efficiently analyze and interpret large, complex financial records. With over three years of experience in big data analytics in the audit domain and leveraging tools like SQL, PySpark, Tableau and Excel on a daily basis, my role includes performing ETL processes, running quality checks, summarizing millions of transactions, aligning them with high-level Balance Sheet/Profit and Loss (P&L) figures across various ERP systems and designing intuitive dashboards that surface meaningful insights which supports critical audit activities such as identifying misstatements, conducting risk assessments, performing threshold checks, and detecting potentially fraudulent patterns enabling faster, more informed data-driven decision-making.

In addition to my core responsibilities, I also lead a small team of junior data analysts—guiding their work, reviewing outputs, and helping them grow their skills while ensuring project quality and consistency.

Whether it's designing customized dashboards for financial use or streamlining cumbersome manual processes, I aim to bring clarity and efficiency to every project. I'm someone who genuinely enjoys solving problems, learning new tools on the fly, and finding smarter ways to do things especially when the clock's ticking.

CREATIVE CORNER

- POEMS

HEALTHTRONICS



-Dr. Jagan Bihari Padhy

ମୁଖଡ଼ା (Chorus)

ଆସ ଆସ ହାତ ମିଳାଇ,
ସୁସ୍ଥ ଜୀବନ ଗୀତ ଗାଇ।
ସଫା ପାଣି, ଶୁଦ୍ଧ ଖାଦ୍ୟ,
ସୁସ୍ଥ ଶରୀର ଆମର ସମ୍ପଦ।
ହସି ହସି ଜୀବନ କାଟିବା,
ରୋଗକୁ ଆମେ ଦୂରେ ରଖିବା।
ଯୋଗ, ବ୍ୟାୟାମ, ପୁଷ୍ଟିକର ଖାଦ୍ୟ,
ସୁସ୍ଥ ଓଡ଼ିଶା ଆମର ଲକ୍ଷ୍ୟ!

ଅନୁରା – ୧ (Nutrition)

ସକାଳୁ ଉଠି ପିଇବା ପାଣି,
ଫଳ ଓ ପରିବା ଖାଇବା ଜାଣି।
ଶାଗ, ଡାଲି ଆଉ ଦେଶୀ ଖାଦ୍ୟ,
ଦେହକୁ ଦିଏ ଶକ୍ତି ଅପାର।
ଜଙ୍କ ଫୁଡ୍‌କୁ କହିବା ନା,
ସ୍ୱାସ୍ଥ୍ୟ ସହିତ କରିବା ହଁ।
ଖାଦ୍ୟ ଥାଳିରେ ରଙ୍ଗ ଭରିବା,
ସୁସ୍ଥ ଜୀବନ ଗଢ଼ି ତୋଳିବା।

ଅନୁରା – ୨ (Exercise & Mental Health)

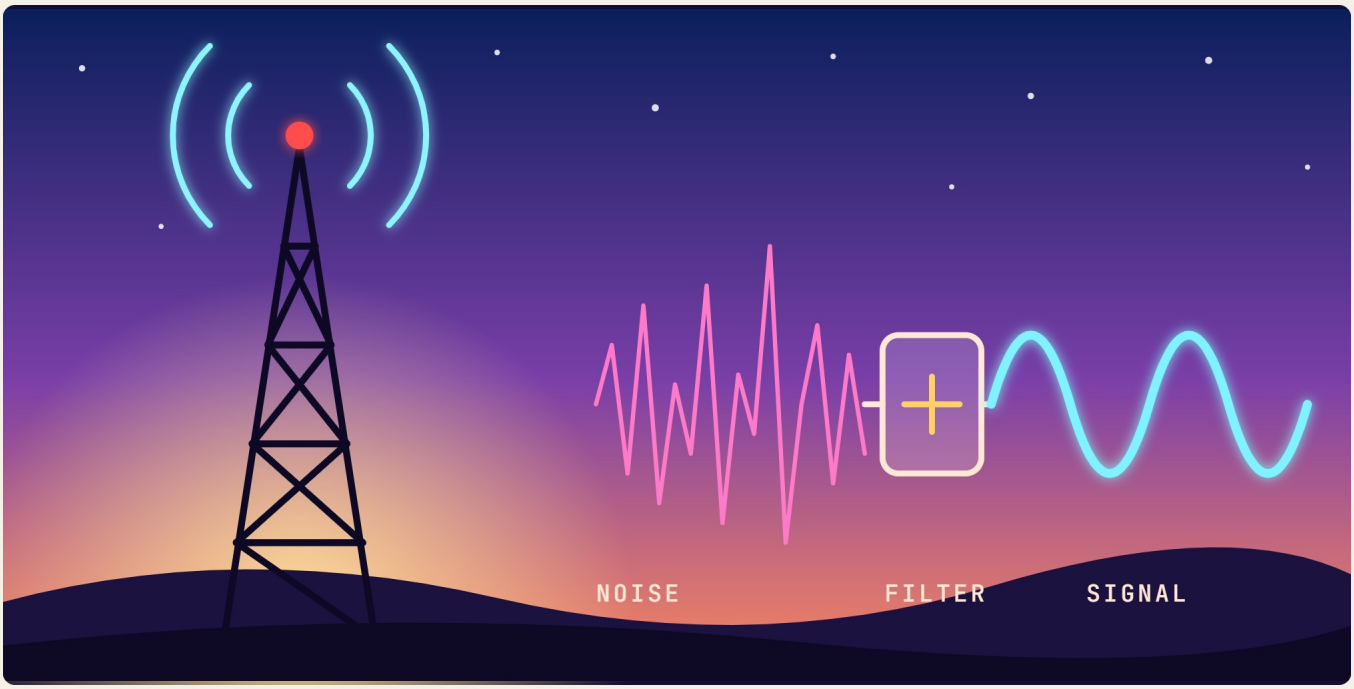
ମୋବାଇଲ୍ ଛାଡ଼ି ପଡ଼ିଆକୁ ଯିବା,
ପ୍ରତିଦିନ ଟିକେ ଦୌଡ଼ି ଆସିବା।
ଯୋଗ ଓ ପ୍ରାଣାୟାମ କରିବା,
ମନର ଚିନ୍ତା ଦୂରେ ରଖିବା।
ହସ ହେଉ ଆମ ଔଷଧ ଭାଇ,
ମନ କଥା କହିବା ଲୁଚାଇ ନାହିଁ।
ଭଲ ନିଦ ଆଉ ଶାନ୍ତ ମନ,
ସୁସ୍ଥ ରଖିବ ଆମ ଜୀବନ।

ଅନୁରା – ୩ (Cleanliness & Prevention)

ହାତକୁ ଧୋଇବା ଖାଇବା ଆଗରୁ,
ସଫା ରଖିବା ଘର ଆମ ଚାରିପାଖରୁ।
ମଶାକୁ ରୋକିବା ପାଣି ନ ଜମାଇ,
ରୋଗକୁ ହଟାଇବା ସଚେତନ ହୋଇ।
ଟିକା ନେବା ସମୟ ଅନୁସାରେ,
ଡାକ୍ତରଙ୍କ ପରାମର୍ଶ ମାନିବାରେ।
ରୋଗ ହେଲେ ନ କରିବା ଡେରି,
ସ୍ୱାସ୍ଥ୍ୟ ହିଁ ସମ୍ପଦ ସବୁଠୁ ବଡ଼ି।

ଅନ୍ତିମ ମୁଖଡ଼ା (Grand Finale)

ଆସ ଆସ ହାତ ମିଳାଇ,
ସୁସ୍ଥ ଓଡ଼ିଶା ଗଢ଼ିବା ଆମେ ଭାଇ।
ଗାଁରୁ ସହର, ଘରରୁ ଦେଶ,
ସ୍ୱାସ୍ଥ୍ୟ ସଚେତନତା ହେଉ ଆମ ବେଶ।
ନିଜେ ସୁସ୍ଥ, ପରିବାର ସୁସ୍ଥ,
ସମାଜ ହେଉ ଆନନ୍ଦମୟ ଓ ସୁସ୍ଥ।
ଆଜିର ସଂକଳ୍ପ, କାଲିର ଆଶା,
ସୁସ୍ଥ ଓଡ଼ିଶା, ସୁନ୍ଦର ଓଡ଼ିଶା!



COMMUNICATION SYSTEMS

Signal in the Noise

On antennas, filters, and the art of being heard.

The air is full of voices none can hear —
a thousand songs that ride the same thin sky.
Your antenna leans in, patient, tuned, sincere,
and lets the million others wander by.

Static hisses, rough as falling rain,
but filters know what matters, what to keep;
they sift the shouting till the line is plain,
and wake a single whisper from its sleep.

So every call that finds its way to me
has crossed a storm of waves to reach my ear —
engineering's quiet poetry:
to make one word, among the noise, ring clear.

ELECTRONIC DEVICES

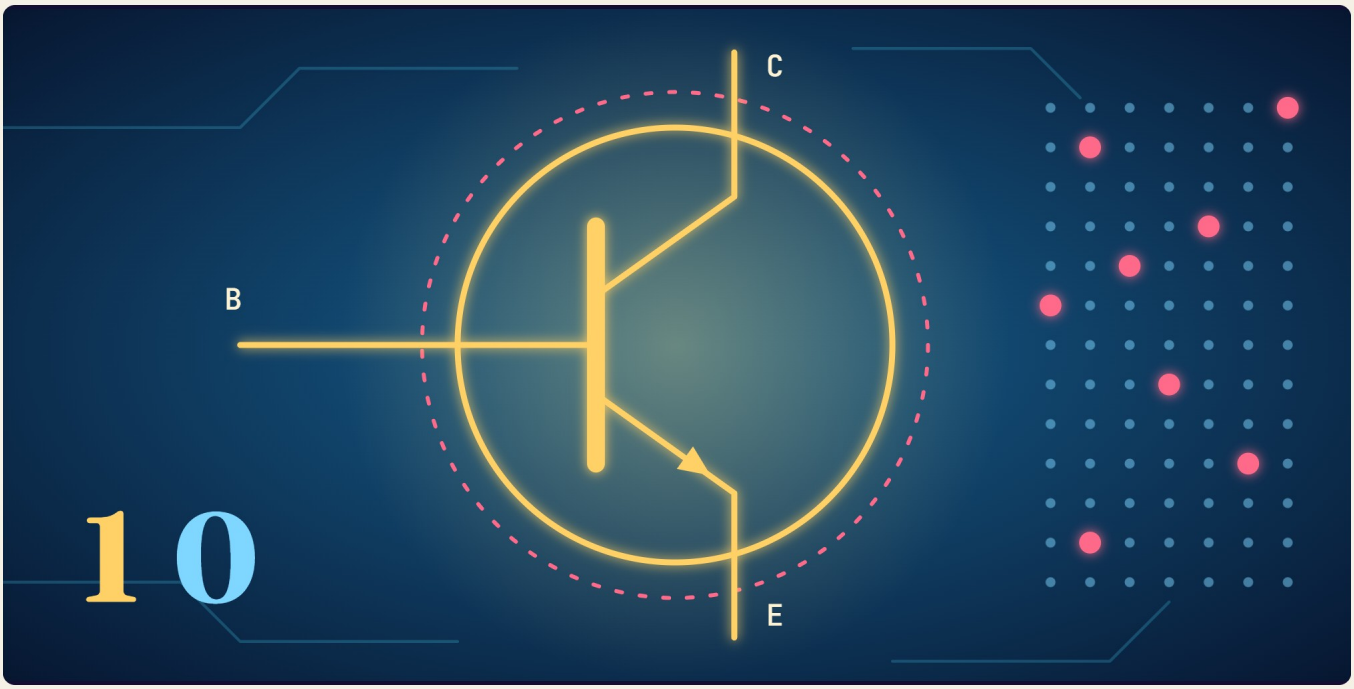
Ode to the Transistor

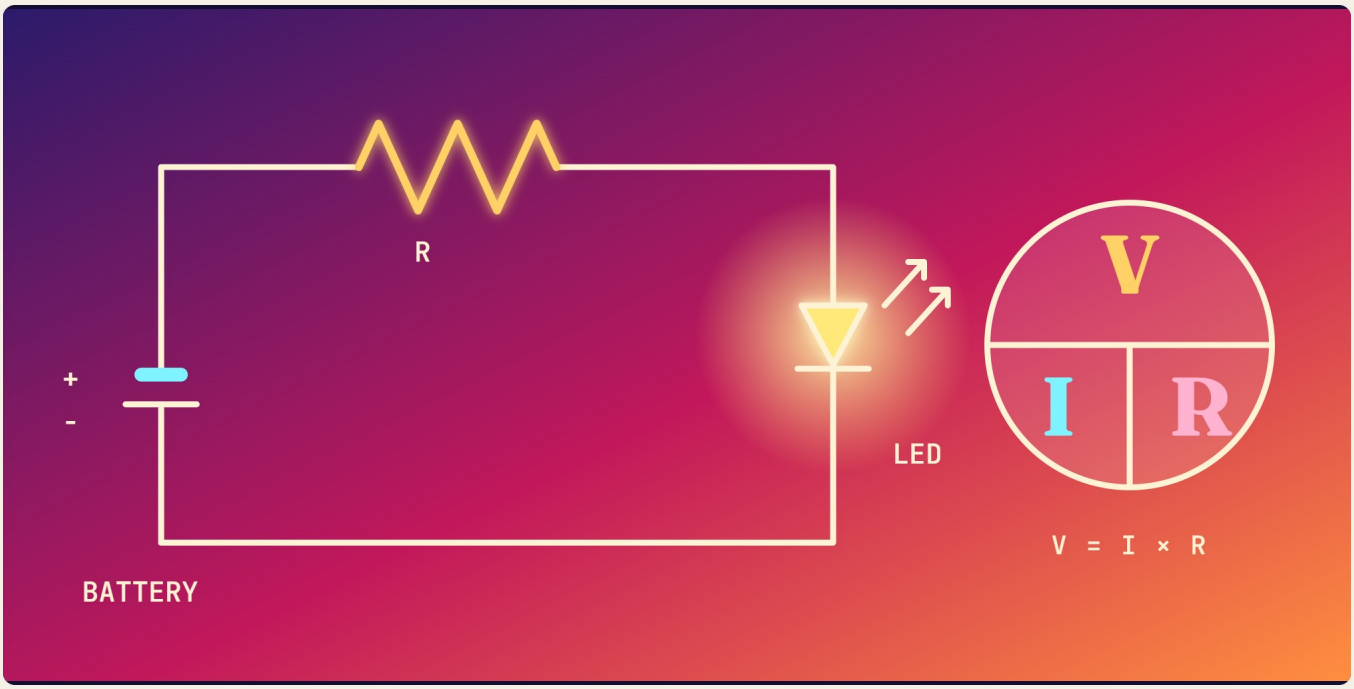
For the smallest switch that ever changed the world.

Smaller than a grain of sand,
you hold a door between zero and one.
Push a little voltage and the door swings wide;
withdraw it, and the dark returns.

Billions of you in the palm of my hand,
each one only a yes or a no,
yet together you keep my mother's voice,
steer a rocket, light a screen at midnight.

Nobody sings of the switch.
So here it is: for every tiny decision
made ten billion times a second
so that I could scroll in peace.





CIRCUIT THEORY

Ohm's Law of Friendship

A lecture-hall daydream in three verses.

V equals I times R, the teacher said,
and wrote it on the board.
I copied it, then drifted off
to think of you instead.

When voltage climbs, as exams do,
the current is your laugh;
the resistance is that 8 a.m. lab
that cuts our sleep in half.

Short circuits? Only deadlines.
Open circuits? Missing notes.
But you are the ground in every lab,
the place where all my panic goes.

ELECTRONICS LAB

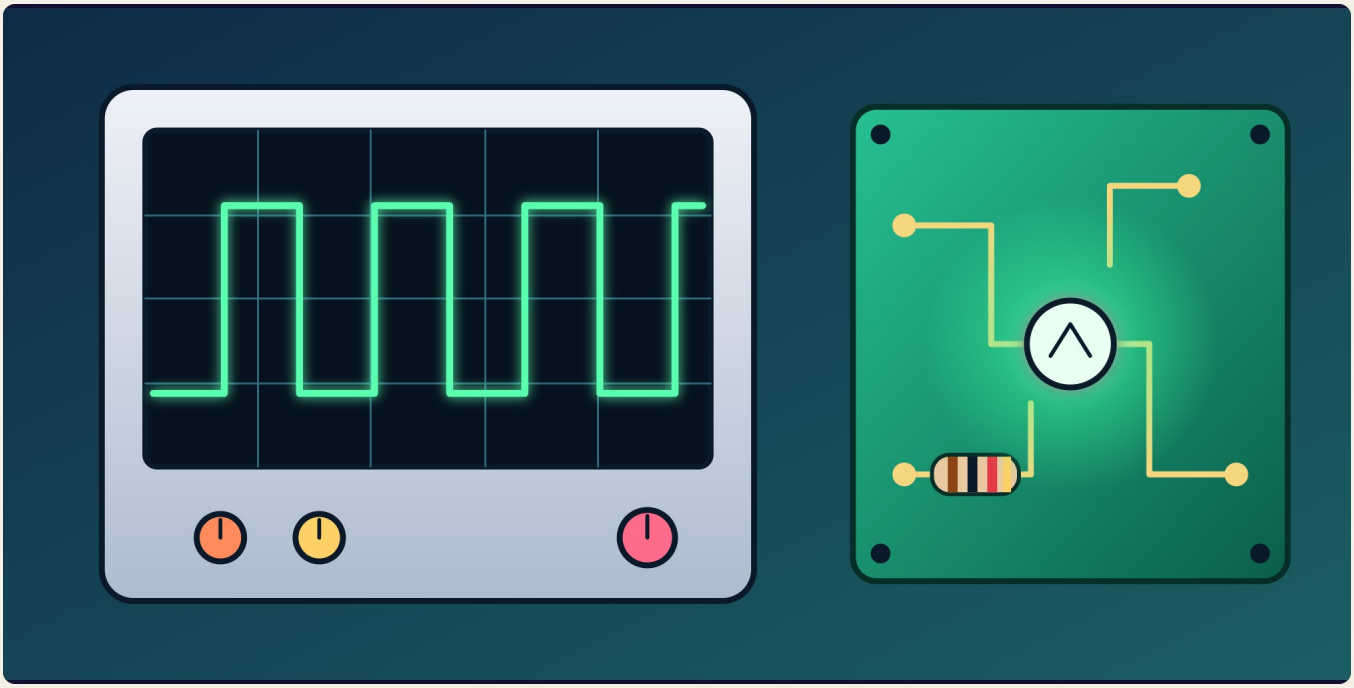
Last Night in the Lab

For everyone who has ever debugged a circuit at midnight.

Midnight hums in the lab's blue light,
the oscilloscope draws a trembling line.
One wire misplaced, one pin not right,
and the whole world refuses to shine.

I trace the board with a tired thumb,
check each joint, each solder bead,
until the LED, stubborn, dumb,
blinks once, as if it had not been dead.

> *Small green heartbeat, steady, slow:*
> *all night's patience, paid in glow.*



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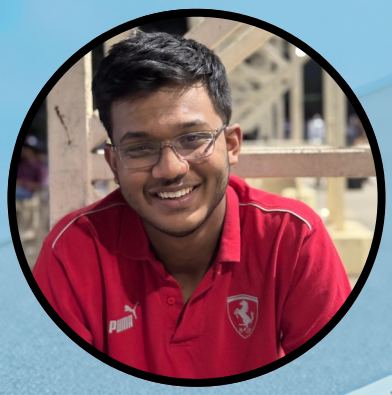

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